A LOW-POWER VIDEO 10-BIT CMOS D/A CONVERTER USING MODIFIED LOOK-AHEAD CIRCUIT

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Abstract—This paper describes a 10 bit 50MSample/s CMOS D/A Converter fabricated in a 1um single-poly double-metal CMOS process. About 30% power could be saved in video application by using a modified look-ahead circuit. The INL is less than 0.46LSB, and the DNL is less than 0.03LSB in the power-save mode. The settling time to 0.1% is less than 20ns. At 50MS/s the SFDR is 60dB. This D/A converter has a single power supply of 5V, and at 50MS/s when the input is all zero dissipates 20mW and all one dissipates 250mW. The core chip size is 1.4mm x 2.8mm.

Index Terms—CMOS D/A converter, video application, modified look-ahead circuit.

I. INTRODUCTION

In digital video signal processing systems, high conversion speed and high resolution CMOS D/A converters are indispensable. The CMOS DAC has the advantages of low power, low cost, I/O compatibility with TTL, and are capable of being integrated with digital processing IC's for video application. Now it is widely used in digital TV, HDTV, MPEG decoding system and the top-box etc.

In the consumer market of video system, integration and programmability are main trends and key requirements, DAC is usually integrated with some DSP digital circuitry. So the motivation to lower the DAC power in different application is obvious.

This paper describes a 10 bit 50MS/s DAC fabricated in a 1um single-poly double-metal CMOS process. A hybrid strategy is adopted using thermometer-code approach for the top 7 MSBs and a binary-scaled technique for the lower 3 LSBs. Here we presented a novel modified look-ahead circuit to reduce the power. In digital video signal like NTSC/PAL, large amount of signal is zero during the blank and synchronization time. The modified look-ahead circuit is designed to switch off the current sources when the input is zero, and pre-detect non-zero input before recovering to the normal operating point. The test results reveal that when the input of this 10-bit DAC is 1023, the supply current is 50mA, but when the input is 0, the supply current is only 4mA. When we test it with a field of normal video signal, about 30% power could be saved.

Fig. 1 shows the basic diagram of the DAC. The 7MSBs are segmented into 127 nonweighted current sources, and the lower 3bit are generated by weighted current sources. The inverters at the input nodes are used for buffering.

II. BLOCK DIAGRAM

Besides oversampling DAC, Nyquist-rate DAC can be roughly categorized into four main types: decoder-based, binary-weighted, thermometer-code, and hybrid. Decoder-based converter is straightforward, but suffers from complex switch design and poor power efficiency. The advantage of the binary weighted approach is simplicity and area efficacy, as no decoding is required. But the matching requirement, especially at major bit transitions, is a problem. A full thermometer-coded approach does not have these problems, as all 1-LSB transitions are produced identically. This architecture intrinsically guarantee the matching, monotonicity and glitch performance. Combining the techniques discussed above, we adopted hybrid design, using segmentation. Usually 5+5 or 8+2 segmentation are popular in 10bit DAC design [4]. Because of the area issue we segment 10 bit into 7MSB and 3LSB[2].

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III. POWER-SAVING CURRENT SOURCE

A. Single supply current source

An ordinary current source is shown in Fig. 2(a). Note the need here for precise time edges of \( \phi \) and \( \delta \). If both logic levels are high simultaneously, \( \text{test} \) is shorted to \( \text{low} \). If both logic levels are low at the same time, the drain of Q1 is pulled high and the circuit takes longer to respond. To avoid the use of two logic driving levels, we connect the gate of Q2 to a DC bias voltage, which is generated by a current source replica, so as to form a...
single supply current source showed in Fig. 2(b). The current is steered to the output through Q2, and thus Q1 and Q3 effectively form a cascade current source when they drive current to the output. To maximize the speed in this converter, the voltage swing at the common connections of the current switches should be small. This design does not use two logic B and B¬, and can therefore be clocked at the maximum rate without the need for precise time edges. Two additional transistors are added to the switching transistors to isolate them from the output lines, reducing charge feedthrough due to parasitic gate-drain capacitance.

B. Modified Look-ahead Circuit

For much of the duration of a video signal, large amounts of the DAC currents are flowing to ground through the \( I_{inr} \) switch, during the Sync tip and back porch times when the input is a chain of zero.

A modified look-ahead circuit is designed to switch off the current sources during these times in order to reduce power. Unlike ordinary look-ahead circuit, which usually switch off the two switch transistors, the modified look-ahead circuit switch off the current source transistor, so as to have a better performance. Compared to ordinary look-ahead circuit, here we don’t need precise time edge and the circuit takes less time to respond, so the sampling rate could be higher. Also the switch noise which disturb the designer is alleviated. When a train of zeros goes to the DAC, the current would normally be steered to \( I_{inr} \) (gnd), however, the nand-gate instead switches off the current source to save power. When the nand-gate detects a “1” arriving at the D input of the flip-flop pipeline stage, it switches on the current source to \( I_{out} \), half clock-cycle before it is required to be switched to \( I_{out} \), in order to give the common node time to settle to its correct value, thereby retaining low o/p glitch. Fig. 4 is the simulation results of the current source, which depicts the principle of the look-ahead circuit. The listed signals are data, clock, clear, \( I_{out} \), \( I_{inr} \) and the common node. The wave form demonstrated the pre-settling of the common node and proper work before and after the data transitions.

It should be noted that this mode causes slight linearity degradation. The experimental result reveals that without invoking the power-saving function the INL is only 0.35LSB. This is because the total DAC current, instead of being fixed, now has a signal-dependent variation. The final test result shows that the INL of the power-saving mode is still less than 0.5LSB.

This DAC is fabricated in a 1µm single-poly double-metal CMOS standard digital process. Special care is given to the layout design to achieve best static and dynamic performance. Full symmetric current source layout is adopted, so that neither mirroring nor 180° rotation of the current source can cause output change of...
current source.

Since there are digital part and analog part in each current source cell, guard ring and different supply is introduced. Fig. 5 shows a die photograph. The core circuit chip area is $1.4\text{mm} \times 2.8\text{mm}$.

V. MEASURED PERFORMANCE

Fig. 6 shows the INL and DNL of this D/A converter. For comparison, the INL and DNL without invoking the power-saving are showed in Fig. 7. Table 1 listed the power supply current in the binary-scaled format and the chip performance is summarized in Table 2.

![Fig. 5 Die Photo](image)

![Fig. 6 DNL and INL](image)

![Fig. 7 DNL and INL without power-saving](image)

**TABLE I**

POWER DISSIPATION OF D/A CONVERTER

<table>
<thead>
<tr>
<th>Input Code</th>
<th>Power Supply Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>16</td>
<td>6</td>
</tr>
<tr>
<td>64</td>
<td>8</td>
</tr>
<tr>
<td>128</td>
<td>11</td>
</tr>
<tr>
<td>256</td>
<td>17</td>
</tr>
<tr>
<td>512</td>
<td>30</td>
</tr>
<tr>
<td>1023</td>
<td>50</td>
</tr>
</tbody>
</table>
TABLE 2
SPECIFICATIONS OF D/A CONVERTER

<table>
<thead>
<tr>
<th></th>
<th>lpm CMOS (2M1P)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>10 bit</td>
</tr>
<tr>
<td>Resolution</td>
<td>50 MSample/s</td>
</tr>
<tr>
<td>INL</td>
<td>0.46 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>0.03 LSB</td>
</tr>
<tr>
<td>Settling time</td>
<td>&lt;20 ns</td>
</tr>
<tr>
<td>SFDR to Nyquist(@50MHz)</td>
<td>60 dB</td>
</tr>
<tr>
<td>Area</td>
<td>1.4mm x 2.8mm</td>
</tr>
</tbody>
</table>

VI. CONCLUSIONS

This paper presents a 10 bit 50MSample/s CMOS D/A Converter for video application, which is fabricated in a 1 μm single-poly double-metal CMOS process. A novel modified look-ahead circuit is designed to achieve low power in video application. This DAC has single power supply of 5V, dissipating 20mW when the input is all zero while 250mW when the input is all one. About 30% power could be saved in video application. The INL is less than 0.46LSB, and the DNL is less than 0.03LSB in the power-save mode. The core chip area is 1.4mm x 2.8mm.

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REFERENCES


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