ECE 485 - Computer Organization and Design

2013 Catalog Data: ECE 485: Computer Organization and Design. Credit 3. Prerequisites: ECE 242, CS 350 and senior standing
This course covers basic concepts and state-of-the-art developments in computer architecture: computer technology, performance measures, instruction set design, computer arithmetic, controller and datapath design, memory systems, pipelining, array processing, parallel processing, multiprocessing, abstract analysis models, input-output systems, relationship between computer design and application requirements, and cost/performance tradeoffs. Students will complete a project implementing a version of multiple-cycle processor. Credit will be given for either ECE 485 or CS 470, but not both. (3-0-3) (P)

Enrollment: Elective course for EE majors.


Coordinator: S. Borkar, Senior Lecturer, Department of ECE

Course goals:
After completing this course, the student should be able to do the following:
1. Use the performance / complexity tradeoffs for defining the RISC instruction set
2. Translate a high level program into RISC instruction set
3. Write a RISC assembler level program including use of subroutines for repetitive tasks
4. Design an Arithmetic and Logic Unit (ALU) Hardware for RISC instruction set
5. Identify the single cycle datapath for execution of RISC instructions
6. Identify the multi cycle datapath on how a typical RISC instruction goes through its five stages
7. Develop the pipelining model and identify the hazards associated with its operation
8. Define the control unit and the associated control signals
9. Implement a control unit in various forms including PLA, Sequential circuits, and microprogram
10. Describe the hierarchical memory system and the cache operation
11. Describe the operation of the non-volatile storage system
12. Describe the basic operation of the I/O and the interconnecting bus
13. Develop and test a VHDL program to capture the processor module operation

Prerequisites by topic:
1. Boolean algebra, Combinational logic designs
2. Basic programming

Lecture schedule: Two 75-minute sessions per week.
Laboratory schedule: None.

Topics:
1. Introduction to Computer Architecture (1 week)
2. Instruction Set Architecture (1 week)
3. MIPS Instruction Set (1 week)
4. Computer Arithmetic (0.5 week)
5. Arithmetic Logic Unit Design (0.5 week)
6. Introduction to VHDL (0.5 week)
7. Computer Performance (0.5 week)
8. Data Path and Control - Single Cycle Operation (0.5 week)
9. ALU Control and Control Logic (0.5 week)
10. Multicycle Datapath Design (1 week)
11. Multicycle Datapath and Control Design (0.5 week)
12. Microprogramming (0.5 week)
13. Pipelining (0.5 week)
14. Pipelining Control and Hazards (0.5 week)
15. Pipelining: Branch Hazards and Exceptions (1 week)
16. Pipelining: Advanced Techniques (1 week)
17. Introduction to Memory Systems (1 week)
18. Cache Fundamentals (1 week)
19. Cache Performance Improvements (0.5 week)
20. Virtual Memory (0.5 week)
21. Storage and I/O Interface (1 week)
22. Tests (1 week)

Computer usage: Students complete a major project of designing and testing a key module, e.g. ALU datapath and microprogram, using VHDL on PCs.

Laboratory topics: None.

Relationship of ECE 485 Course Goals to Student Outcomes:

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<tr>
<th>Student Outcomes:</th>
<th>Course Goals</th>
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<tbody>
<tr>
<td>a. Apply knowledge of math, engineering, science</td>
<td>1, 2, 3, 4, 9, 13</td>
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<td>b. Design and conduct experiments / Analyze and Interpret Data</td>
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<td>c. Design system, component, or process to meet needs</td>
<td>4, 5, 6, 8, 9, 13</td>
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<td>d. Function on multi-disciplinary teams</td>
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<td>e. Identify, formulate, and solve engineering problems</td>
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<td>f. Understand professional and ethical responsibility</td>
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<td>g. Communicate effectively</td>
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<td>h. Broad education</td>
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<td>i. Recognize need for life-long learning</td>
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<td>j. Knowledge of contemporary issues</td>
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<td>k. Use techniques, skills, and tools in engineering practice</td>
<td>4, 7, 9, 10, 11, 12, 13</td>
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Prepared by: S. R. Borkar Date: Oct 16, 2013