ECE 429 - Introduction to VLSI Design

Processing, fabrication, and design of Very Large Scale Integration (VLSI) circuits. MOS transistor theory, VLSI processing, circuit layout, layout design rules, layout analysis, and performance estimation. The use of computer aided design (CAD) tools for layout design, system design in VLSI, and application-specific integrated circuits (ASICs). In the laboratory, students create, analyze, and simulate a number of circuit layouts as design projects, culminating in a term design project. Prerequisites: ECE 218, ECE 311, senior standing. (3-3-4) (P) (C)

Enrollment: Elective course for EE majors; hardware-design elective course for CPE majors.


Coordinator: J. Wang, Assistant Professor of ECE

Course goals:
After completing this course, the student should be able to do the following:
1. Design VLSI circuits from register-transfer level to layouts.
2. Discuss the basic attributes of VLSI systems, their impact upon society, and the tradeoffs between design metrics, especially speed, power, and cost.
3. Design experiments to measure design metrics and explain the differences between theoretical models and experiments.
4. Identify the basic parts of VLSI design flows. Compare/contrast both custom and standard-cell based design methodologies.
5. Explain and analyze dynamic techniques such as charge sharing and current leakage and how it impacts specific circuits from a dynamic circuits perspective.
6. Complete an engineering design incorporating engineering standards and realistic constraints.
7. Prepare an informative and organized design project report with solid supporting data and deliver an oral presentation.

Prerequisites by topic:
1. Familiarity with logic gates and digital systems.
2. Knowledge of microelectronic circuits.

Lecture schedule: Two 75-minute sessions per week
Laboratory schedule: One 160-minute session per week

Topics:
1. MOS Transistor Theory (1 week)
2. CMOS Fabrication, Layout, Processing Technology (1 week)
3. Logical Effort (1 week)
4. Delay and Power Estimation for CMOS (1 week)
5. Interconnect and wire engineering (1 week)
6. Simulation in HSPICE and Verilog (1 week)
7. Combinational Circuit Design (1.5 week)
8. Sequential Circuit Design (1.5 week)
9. Adders (1.5 week)
10. Datapath Functional Units (1 week)
11. Memories (1 week)
12. Final project and Demonstration (1 weeks)
13. Midterm and Final Exams (1.5 weeks)

Computer usage:
Students use industrial design tools from major vendors (Synopsys, Cadence, and Mentor Graphics) on Unix and Linux systems in the lab assignments and the final project.
Laboratory topics:
1. Lab Setup (1 week)
2. Inverter Schematic (1 week)
3. Inverter Layout (1 week)
4. Gate Delay and Power (1 week)
5. Hierarchical Design and Formal Verification (1 week)
6. Carry-Ripple Addition I (1 week)
7. Carry-Ripple Addition II (1 week)
8. Carry-Ripple Addition III (1 week)
9. ASIC Design Flow (1 week)
10. Final Project: Design and Synthesis of Central Processing Units (4 weeks)

Relationship of ECE 429 Course Goals to Student Outcomes:

<table>
<thead>
<tr>
<th>Student Outcomes</th>
<th>Course Goals</th>
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<tbody>
<tr>
<td>a  Apply knowledge of math, engineering, science</td>
<td>1,2,3,4,5,6</td>
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<td>b  Design and conduct experiments /Analyze and interpret data</td>
<td>3,6</td>
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<td>c  Design system, component, or process to meet needs</td>
<td>1,6</td>
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<td>d  Function on multi-disciplinary teams</td>
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<td>e  Identify, formulate, and solve engineering problems</td>
<td>1,5,6</td>
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<td>f  Understand professional and ethical responsibility</td>
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<td>g  Communicate effectively (written / oral)</td>
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<td>h  Broad education</td>
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<td>i  Recognize need for life-long learning</td>
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<td>j  Knowledge of contemporary issues</td>
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<td>k  Use techniques, skills, and tools in engineering practice</td>
<td>4,6</td>
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Prepared by: J. Wang  
Date: October 15, 2013