Design and Simulation of a 5GHz Distributed Amplifier

A high performance, low-cost distributed amplifier for use in a CATV system

Philip Felber • Brian Tierney • Yves Vaillant

ECE-524 Electronic Circuit Design

May 1, 2000

PART I : Introduction & Background

A. THE PRESENT NEED FOR DISTRIBUTED AMPLIFICATION

The amplifier described in this paper is intended for use as the power amplifier stage of a CATV distribution amplifier, with a bandwidth extending to a frequency range of several gigahertz (GHz).

The common CATV amplifier in use today, though, is not a distributed amplifier. It has its limitations, as the need for bandwidth keeps increasing. Present day CATV amplifiers are push-pull or power-doubler Class A hybrids (integrated low level circuits plus discrete devices for the power amplifier). Today, CATV signals are received via a hybrid fiber coax (HFC) network. However, the last several hundred feet to the end user is still (and will be for several years) coaxial cable. Although transmission line theory predicts that coaxial cable can operate at infinite bandwidth, the reality is different.

In transmission line theory, if the product of the line resistance (R) times the capacitance (C) is equal to the line conductance (G) times the inductance (L), the attenuation should be independent of frequency. Yet, the loss in real coaxial cable increases with frequency. Each of the R, C, G, and L elements actually has a small frequency dependence, not the least of which is the AC resistance or "skin effect" that causes R to increase with frequency. To compensate for the increase loss in coax at high frequencies, CATV amplifiers are generally designed with an adjustable frequency response. A positive slope in the amplifier imparts a frequency tilt to the signals passing through it, so that the higher frequency channels are at higher power levels than the lower frequency channels to offset the increased high frequency attenuation.

The demand for more channels (i.e., bandwidth) will never cease. The 6 MHz channel has become the CATV unit of bandwidth. One channel (unit of spectrum) can contain one conventional analog TV program in National Television Standards Committee (NTSC) format. A single channel could also be used to transmit about a dozen (TV quality) television programs or about 30 (Compact Disk quality) stereo high fidelity sound programs. Also, each 6 MHz channel can support many Internet users surfing the World Wide Web (WWW). Of course, several channels could be coupled together to handle a program or service that requires more than 6 MHz of bandwidth. Furthermore, although the coax that is in use has a very high attenuation at the GHz frequencies, adequate power can be provided to make the spectrum up to several GHz usable. We get some help by sloping the CATV amplifiers and there is less man made interference (the high power broadcast TV transmitters now use the very high frequency (VHF) range). The frequencies above about 600 MHz will be used for digital service (Digital TV and Internet). The current digital protocols only need about 15 decibels (dB) of signal to noise ratio (SNR), while our conventional analog TV needs about 55 dB for a good picture.

Clearly then, there will be a market for an inexpensive CATV amplifier to accommodate the very large bandwidth of 50 MHz to 5 GHz. As will be shown, the distributed amplifier can do the job!

B. A BRIEF HISTORY OF DISTRIBUTED AMPLIFICATION

Dr. W. S. Percival (1937 patent) is credited with inventing the distributed amplifier. The name "distributed amplifier" was coined by Dr. Edward L. Ginzton in a 1948 Institute of Radio Engineers (IRE) paper. The first use of this distributed amplifier technology in the Cable TV Industry was in the Spencer Kennedy Laboratories Model 212-C broadband chain amplifier (about 1954). Prior to this time, single channel strip amplifiers were used for each 6 MHz channel.

Of course, all electronics from that era employed vacuum tubes. By the late 1950s though, as vacuum tubes were being replaced by bipolar junction transistors (BJT), tubes survived only in niche applications, such as wideband distributed amplifiers. (The BJT is basically a low to medium impedance device, and as such, is not very compatible with distributed amplifier theory). The end result was that the distributed amplifier was forgotten by most engineers (as solid-state design provided more lucrative employment !), and are thus not widely used in present CATV amplifiers.

The development of the field effect transistor (FET) in the 1960s, followed by the integrated circuit (IC) in the 70s, sparked a renewed interest in the distributed amplifier because, FETs, like tubes, have an ideally infinite input impedance. By 1980 there were off the shelf (OTS) Gallium Arsenide (GaAs) distributed amplifiers, and today, we are seeing low-cost CMOS-based completely integrated distributed amplifiers operating up to and beyond 10 GHz.

C. THEORETICAL ADVANTAGE OF DISTRIBUTED AMPLIFICATION

Distributed amplifier technology breaks the usual *gain x bandwidth = constant* product limit that is a bottleneck when high frequencies *and* significant power gain are both needed.

a. How does it work?

First, consider the following Class-A amplifier:

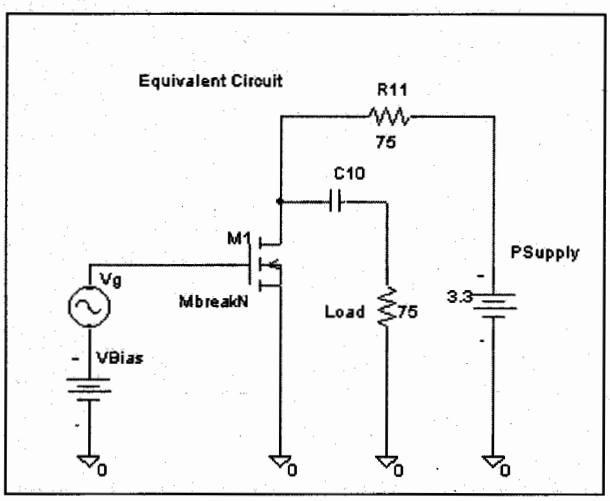


FIGURE 1.

The gain x bandwidth product of such an amplifier is governed by the ratio

$Gain * Bandwidth = \frac{gm}{2\pi * C}$, as found from the following small signal model:

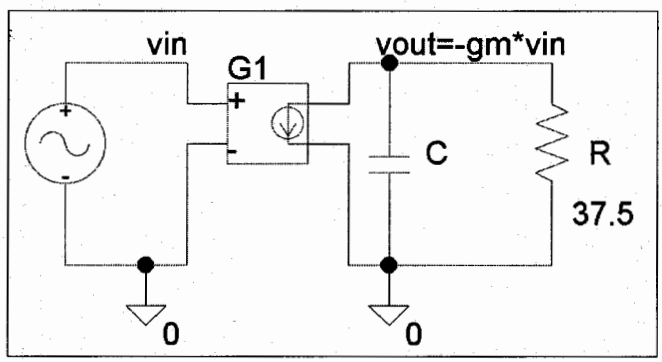


FIGURE 2.

(*Note:* The C10 capacitor of Fig. 1 is a coupling capacitor and is not represented in the AC analysis). C in fig 2. incorporates both the effects of C_{gd} and C_{gs}, as will be discussed later.

To illustrate the effect of this constant gain bandwidth product, we shall consider four class A amplifiers in parallel. In this case, the equivalent capacitance is four times C. We keep the same load R, therefore the bandwidth is 4 times smaller: $f_c = \frac{1}{4} * \frac{1}{2\pi RC}$, but the overall gain is now: $A_v = -4 * gm * R$.

For the case of the distributed amplifier, though, unlike the above case where adding parallel stage transistors causes the capacitances to add and results in bandwidth reduction, the distributed amplifier prevents the parasitic capacitance of each stage from summing together. As the gain increases for each stage that is added, the "amplifier as a whole", only sees the "effective capacitance" of one stage. Thus the Gain x BW product can rise, and not remain constant. This capacitor non-additive effect occurs by distributing the parasitic capacitances in a transmission line. The basic topology is as such:

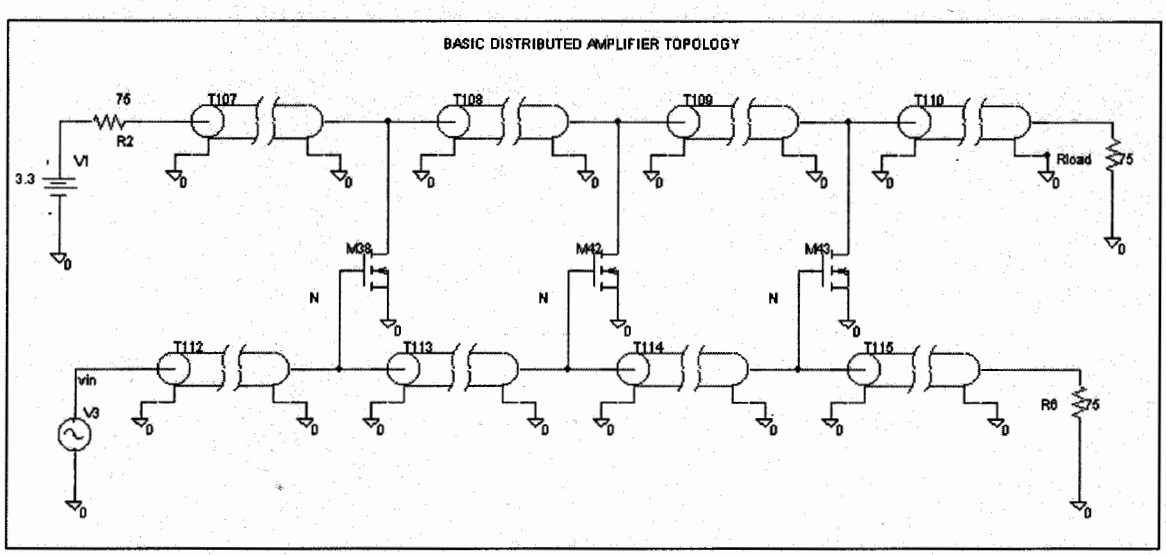


FIGURE 3.

b. Simulations

Using the schematic in Figure 3, a PSPICE comparison of the four Class A stages amplifier topology vs. a four Class A stages distributed amplifier topology has been done. Refer to the ideal distributed amplifier schematic and voltage gain plot (Figures 4 and 5, respectively).The plot in Fig. 5 compares the constant Gain x Bandwidth product seen for the single and 4 parallel stage amplifiers vs. the bandwidth enhancement obtained using the distributed topology.

Figure 4.

Distributed Amplification Versus Classical Parallel Stage

Equivalent study circuits

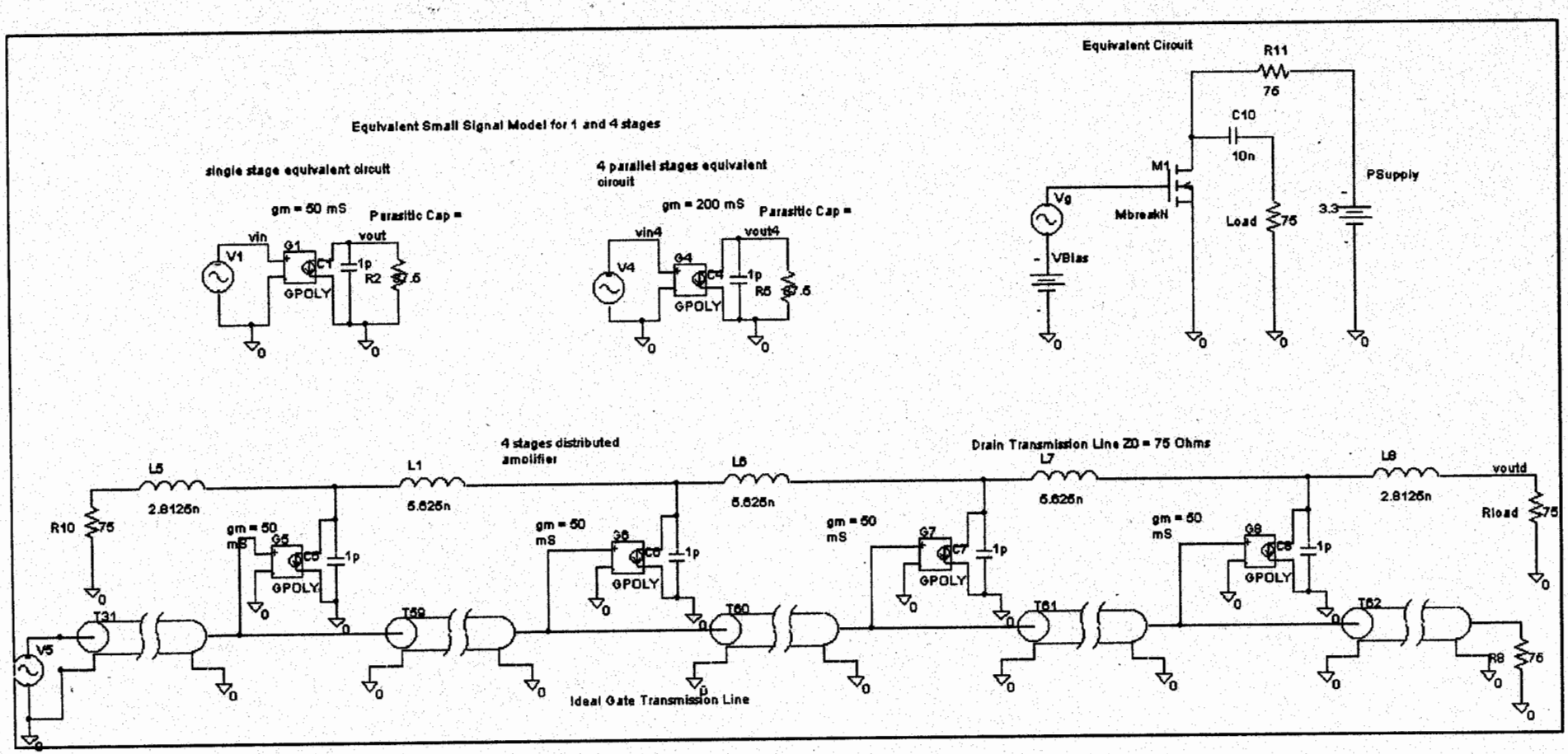
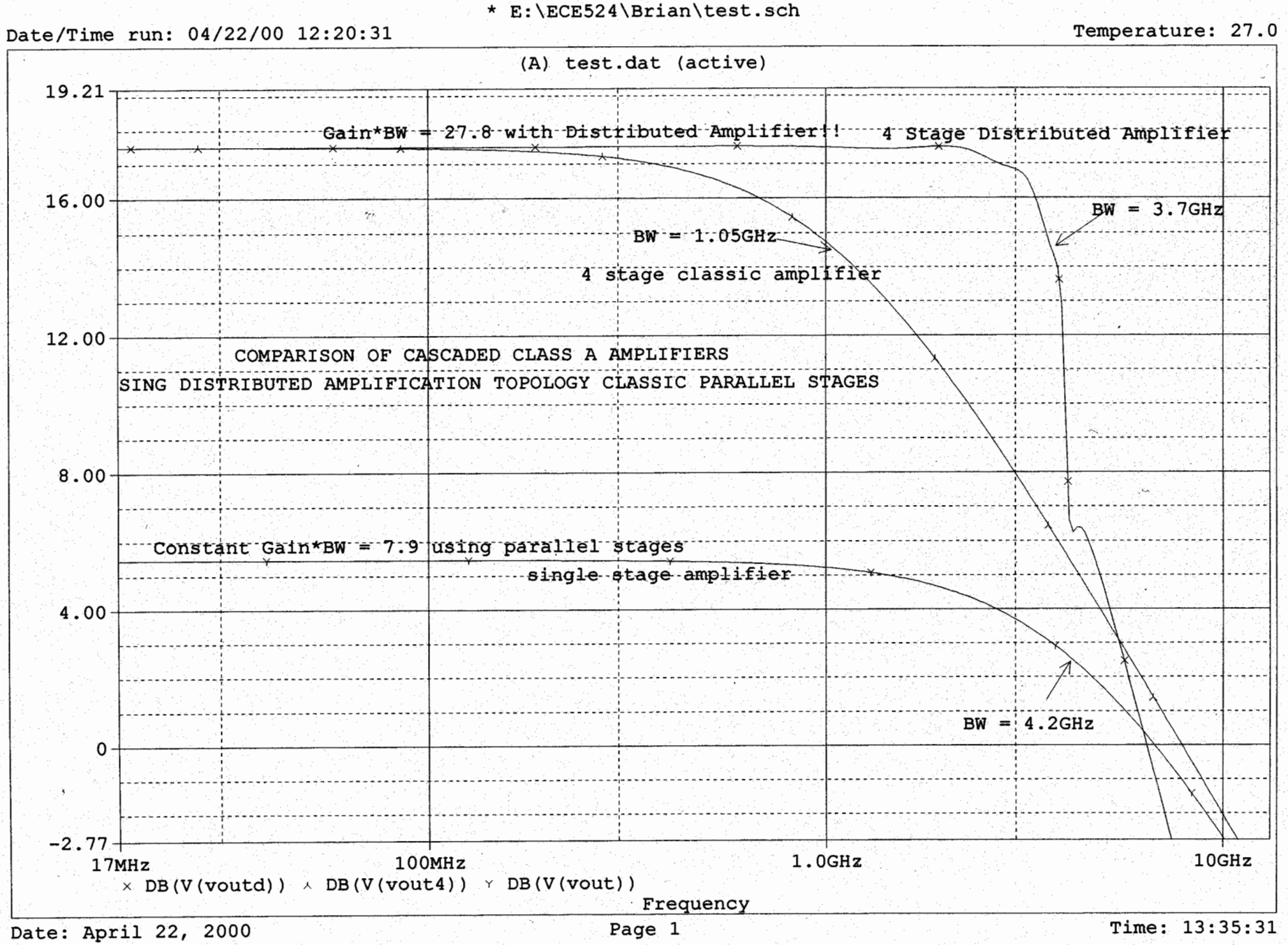


Figure 5. Comparison of Parallel Class A stages vs. Distributed Amplifier



It can be clearly seen that a 350% bandwidth increase is obtained with the distributed case, with the same gain as in the 4 parallel stages case. Therefore, the distributed amplifier will allow significant power to be delivered to the 75Ω load at higher frequencies.

PART II : CONSTRUCTION OF OUR DISTRIBUTED AMPLIFIER

A. Design Flow – A chronology

Now, all the subsections of our final design will be presented, as they were chronologically derived (for the sake of clarity). This process involved much trial and error. We shall conclude by presenting the final realization as well as a comparison between the theory and the measurements.

Our original schematic, shown below, is an extension of the single class A stage amplifier discussed above.

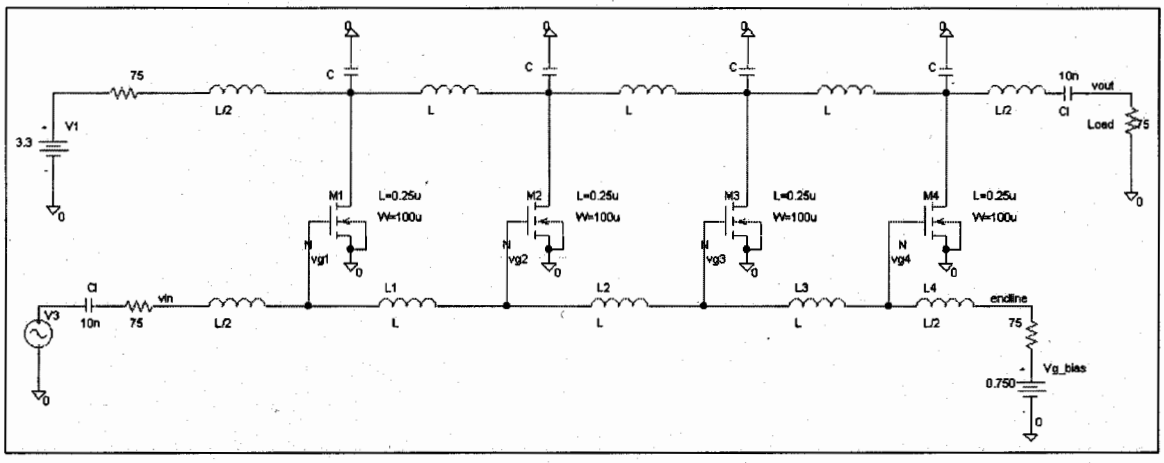


FIGURE 6 – Original distributed amplifier schematic.

a. Realization of transmission line with lumped components

The transmission line is represented by a series connection of π - model *matched* sections:

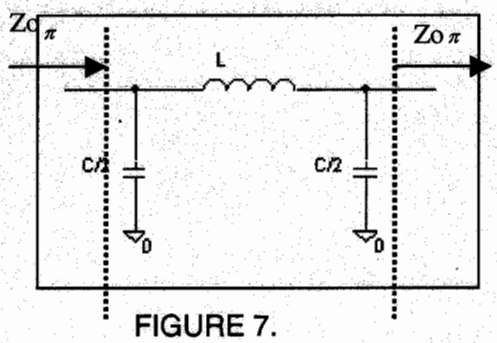


FIGURE 7.

The characteristic impedance of this model is given by: $Zo_\pi = \sqrt{\frac{L}{C}} \frac{1}{\sqrt{1-\frac{\omega^2}{\omega^2_c}}}$

Based upon the single Class A stage gain equation $A_v = -gm * Z_{eq}$, the distributed amplifier gain is given by the equation:

$$A_v = \frac{-N * gm}{2\sqrt{1-\omega^2/\omega^2_c}} \sqrt{\frac{L}{C}} e^{-N*\theta}$$

where :

N = the number of stages.

gm = transconductance of each stage (assuming all transistors equal).

ω_c = cutoff frequency of the gate and drain transmission lines (assumed equal).

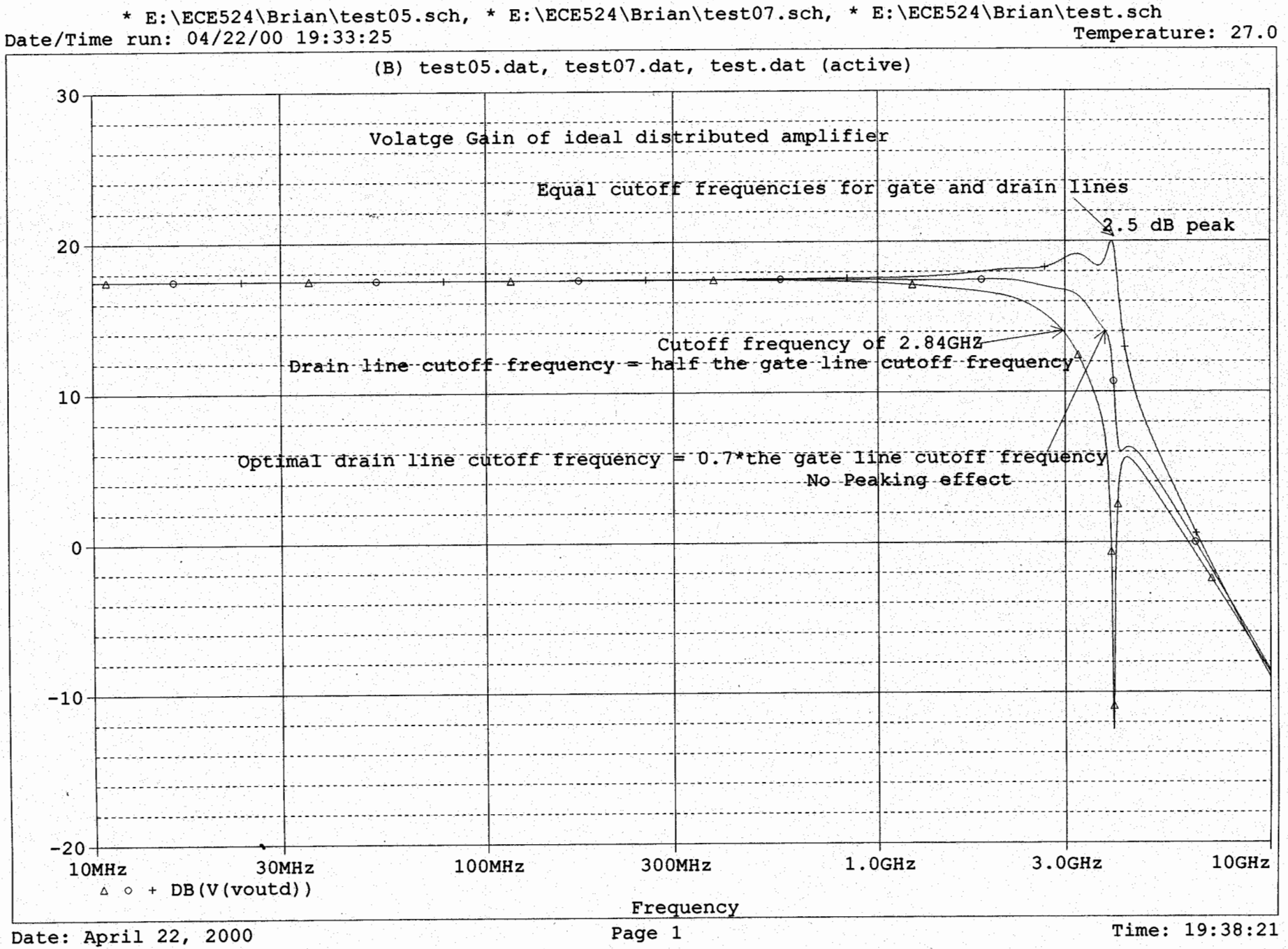
θ = propagation constant of the transmission line, which is, in our case, $j\omega\sqrt{LC}$.

In this expression, $Z_{eq} = \frac{Zo_\pi}{2}$. The factor of ½ is due to the fact that the drain current splits into two π-matched sections.

b. Gain response -- Problem and solution

The term $\sqrt{1-\frac{\omega^2}{\omega^2_c}}$ will cause a peak in the gain as the frequency approaches the cutoff frequency. To eliminate this undesired peaking effect, the drain line cutoff frequency should be slightly smaller than that of the

Figure 8. Comparison of *k* values for Ideal Distributed Amplifier



gate transmission line. By doing this, the drain line will already be 'turned off' by the time the gates of the transistors reach the peak voltage level.

It turns out that the optimal $k = \frac{f_{cdrain}}{f_{cgate}}$ coefficient is 0.7, so that we get the maximum bandwidth without getting any peak in the gain response. A comparison of the voltage gain with several values of *k* of the ideal distributed amplifier is shown in Figure 8.

c. Choosing gate and drain line capacitances

The equivalent capacitance seen from the gate can be obtained using the following network:

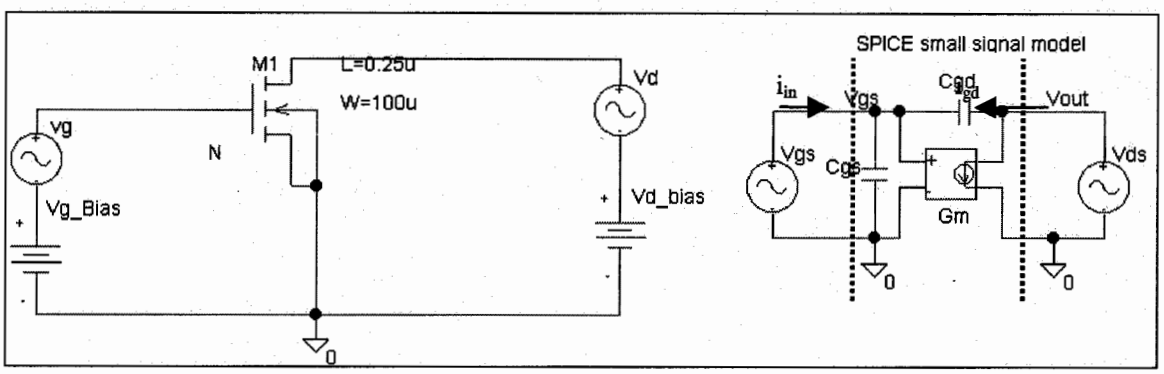


FIGURE 9.

This single stage, taken from the distributed amplifier, was used to determine the equivalent gate and drain capacitances, and hence the line inductances. Once these values were found, they were incorporated in the π-model, as will be explained later.

The bias has been carefully chosen for this single stage, so that the transistor operates exactly at the same Q point as in the distributed case, and the output voltage swing is maximized (using its VTC curve).

From the small signal model, the equivalent capacitance seen from the gate is derived:

$$i_{in} = C_{gs}s * v_{gs} + (v_{gs} - v_{out})C_{gd}s$$

$$\frac{i_{in}}{v_{gs}} = C_{gs}s + (1 - \frac{v_{out}}{v_{gs}})C_{gd}s \qquad \text{where } A_v = \frac{v_{out}}{v_{gs}}$$

$$\Rightarrow C_{eq,Gate} = C_{gs} + (1 - A_v)C_{gd}$$

The AC voltage sources were set so that $A_v = 1$, so that $C_{eq} = C_{gs}$.

Then the same voltage sources were set so that $A_v = 0$,so that $C_{eq} = C_{gs} + C_{gd}$.

Thus, with these two C_{eq} measurements, C_{gd} and C_{gs} are determined for a specific bias.

In a similar fashion, the equivalent capacitance seen from the drain was also derived:

$$i_{gd} = (v_{out} - v_{gs})C_{gd}s$$

$$\frac{i_{in}}{v_{out}} = (1 - \frac{v_{gs}}{v_{out}})C_{gd}s$$

$$\Rightarrow C_{eq,Drain} = (1 - \frac{1}{A_v})C_{gd}$$

d. Derivation of drain and gate π - section parameters

Gate Line π - section:

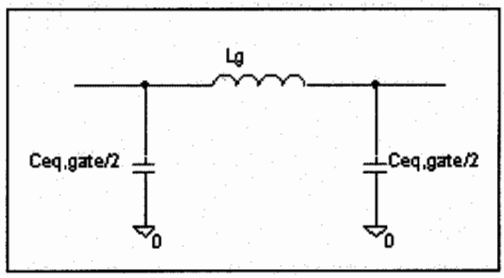


FIGURE 10.

The equations for the gate line π - section are as follows:

f_{cg} = gate line cutoff frequency $= \frac{1}{\pi\sqrt{L_g C_{eq,gate}}}$,

where the cutoff frequency is defined as the frequency at which the equivalent impedance of the section becomes imaginary.

Zo = characteristic impedance of the lines $= \sqrt{\frac{L_g}{C_{eq,gate}}} = 75\Omega$ (load impedance).

T_g = propogation time of a one section $= \sqrt{L_g C_{eq,gate}}$.

Hence, $L_g = Z^2{}_0 * C_{eq,gate}$.

Drain line π - section:

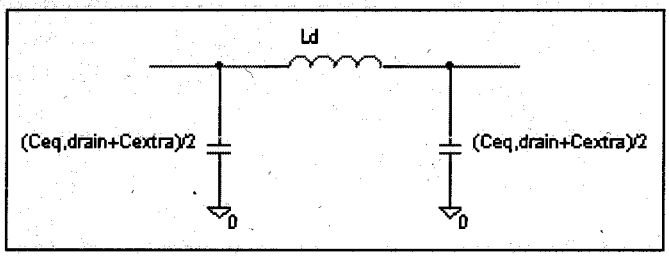


FIGURE 11.

C_{extra} is an external capacitance that is added to the drain line and can be set to match both the characteristic impedance and to obtain a smaller drain cutoff frequency. In this case, C_{extra} is chosen so that *k* equals 0.7. The equations for the drain line π-section are as follows:

f_{cd} = drain line cutoff frequency $= \dfrac{0.7}{\pi\sqrt{L_g C_{eq,gate}}} = \dfrac{1}{\pi\sqrt{L_d (C_{eq,drain} + C_{extra})}}$.

Zo = characteristic impedance of the lines $= \sqrt{\dfrac{L_d}{C_{eq,drain} + C_{extra}}} = 75\Omega$ (load impedance).

T_d = propagation time of a one section $= 0.7\sqrt{L_g C_{eq,gate}} = \sqrt{L_d (C_{eq,drain} + C_{extra})}$.

L_g and $C_{eq,drain} + C_{extra}$ can be chosen to be: $L_d = \dfrac{L_g}{0.7}$, $C_{eq,drain} + C_{extra} = \dfrac{C_g}{0.7}$.

Hence, the extra capacitance is given as $C_{extra} = \dfrac{C_g}{0.7} - C_{eq,drain}$.

B. Bandwidth enhancement -- Matching sections

A transmission line can be terminated with an inductance or capacitance as shown below using a 'T' or π-section:

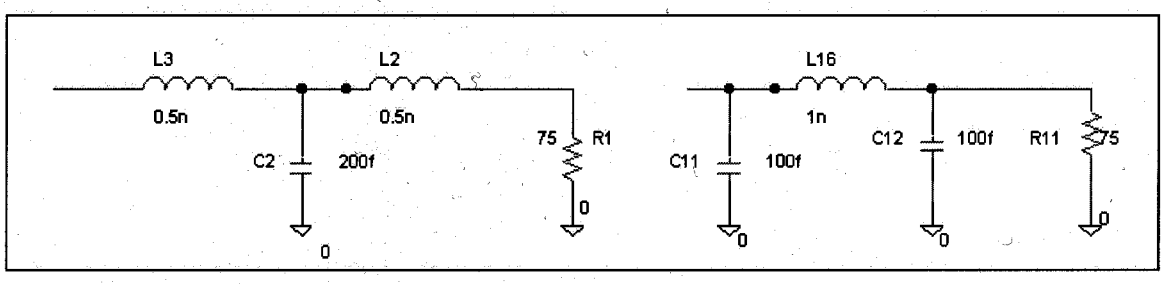


FIGURE 12.

However, to increase the impedance matching with frequency, an m-derived half section was used. This half section has twice the cutoff frequency of a 'T' or π-section and thereby provides a better impedance matching with frequency. A comparison of the 'T' and π-sections shown below in Figure 13, matched using a single resistive load and m-derived half section combination, was made using our latest component values. Refer to Figure 15.

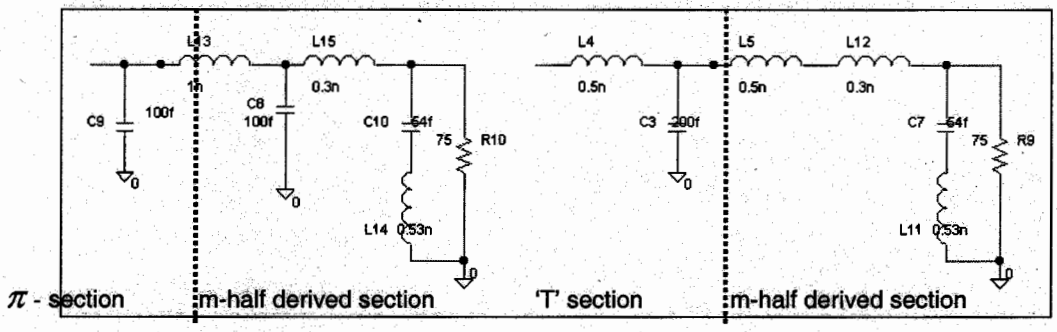


FIGURE 13.

The terminations of the gate and drain lines have been made with 'T' sections using m-derived half sections. The schematic of an m-derived half section is given below:

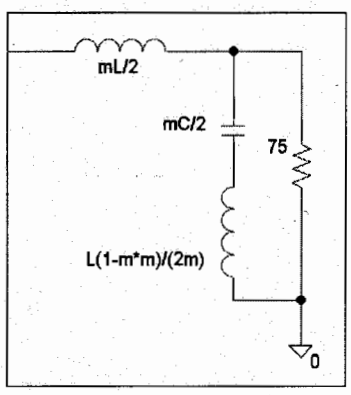


FIGURE 14.

where $L = L_g$ or L_d and $C = C_{eq,gate}$ or $C_{eq,drain+}$ C_{extra} .

Several values of m can be used. In theory, a smaller m gives a better matching with frequency. However, for practical realizations, a value of m = 0.6 is preferred. A 5% tolerance is taken as a reference. Figure 16 compares output voltages at various m values. Note that the frequency where the tolerance is reached is increased by 50%, from 5.4GHz with m = 1, to 8.2 GHz with m = 0.6.

Figure 15. Comparison of T and Pi section terminations

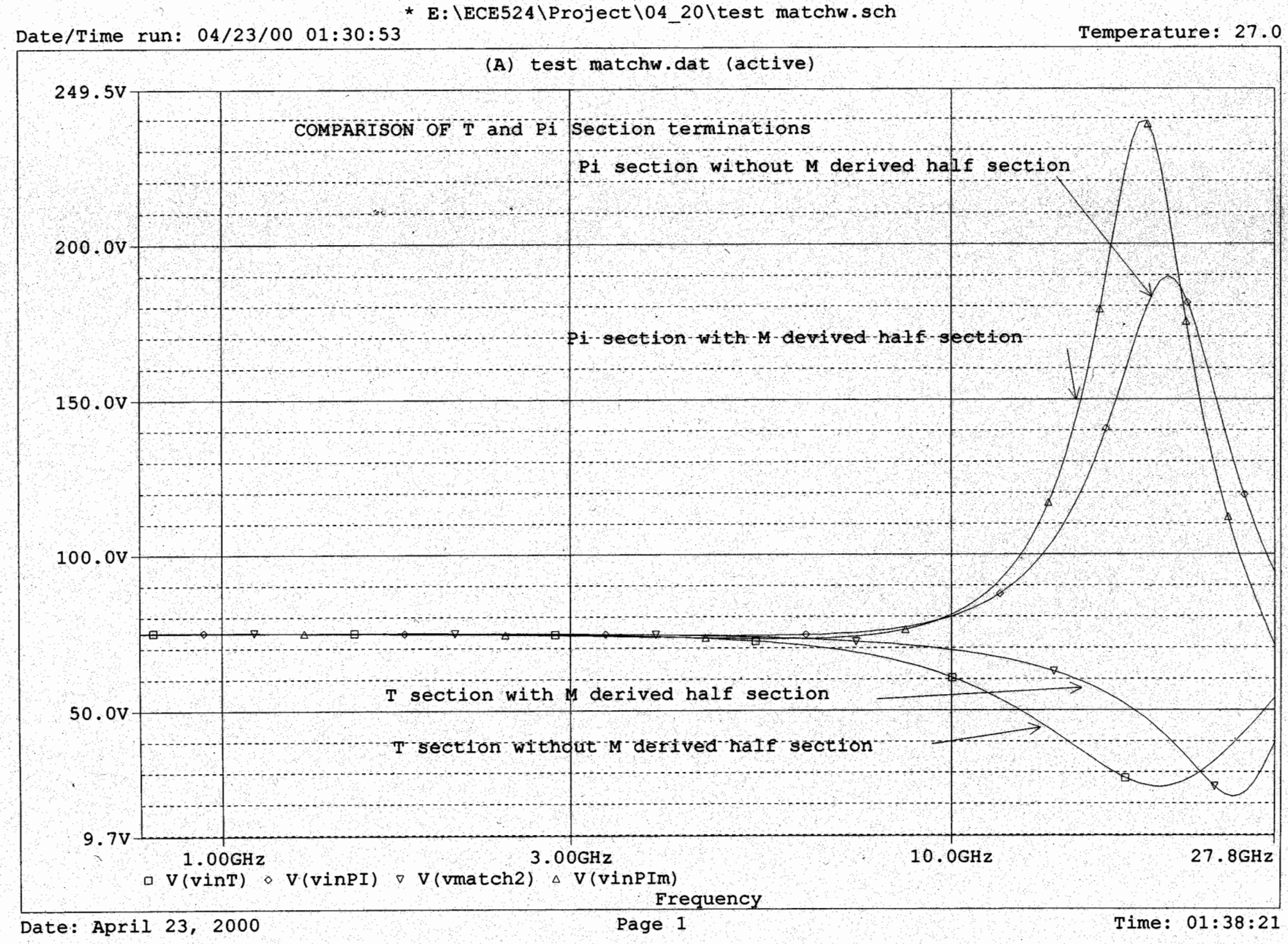
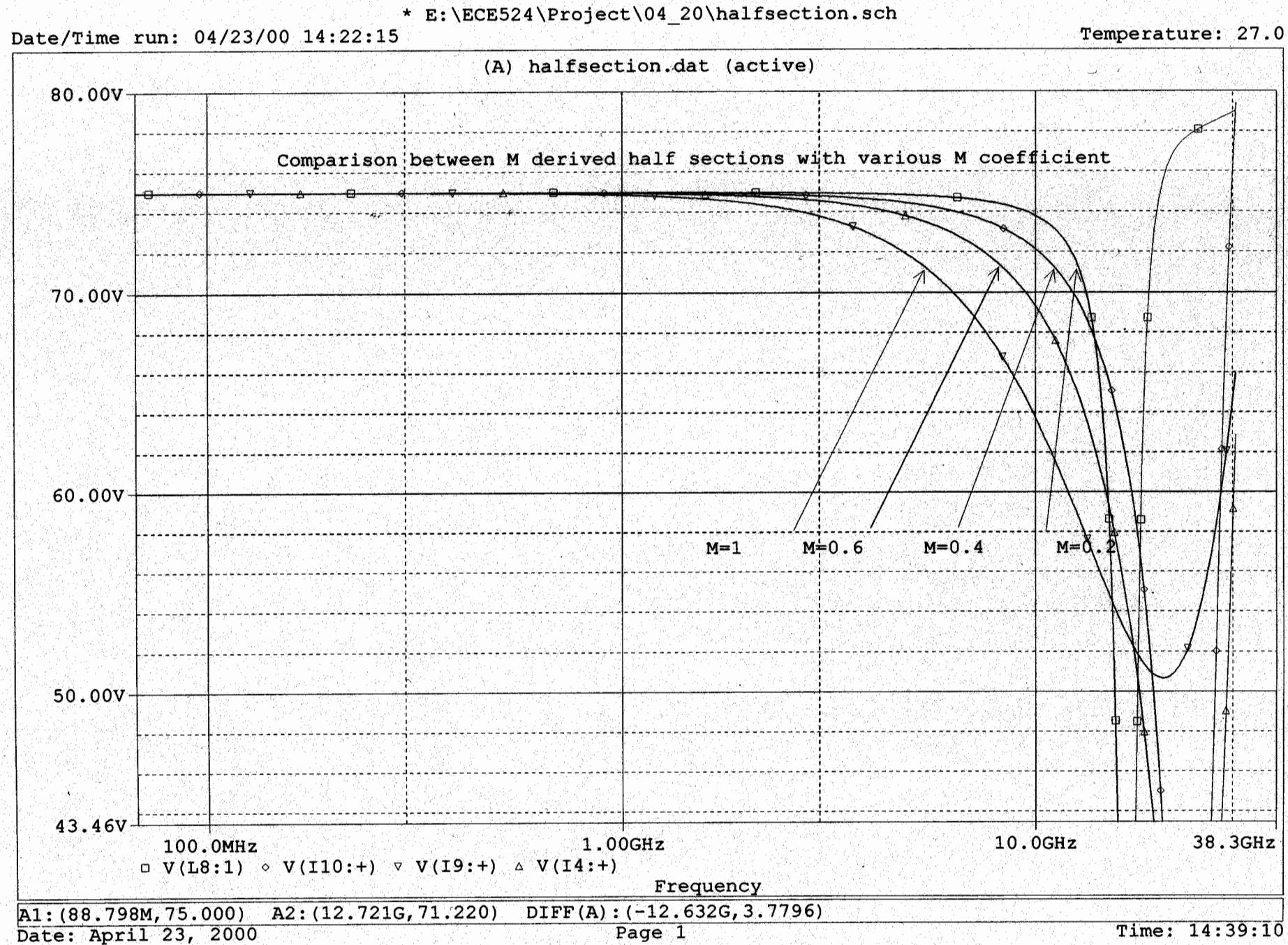


Figure 16. Comparison of m coefficients



C. Increasing the gain – Tapered line topology

a. How can *all the power* be delivered to the load?

If the basic topology of a distributed amplifier is analyzed, it is easily shown that only half of the power is delivered to the load. This is because each current source (i.e., drain source branch) sees two impedances of 75Ω in parallel and, therefore, equal amounts of current flow both ways. As the drain line is assumed matched at both ends, no reflection will occur.

The idea of the tapered line is to deliver all the output currents into the load. For this, a BFL inductance is needed to ensure the proper bias of the transistors. For AC signals it will behave as an open circuit. Hence, we get twice the amount of power to the load. However, with a BFL inductance at the drain line termination, reflection will occur, giving rise to a transient regime. It is then necessary to modify the characteristic impedance of each piece of transmission line so that this transient behavior is as short as possible.

A simple basic schematic is given next to illustrate the advantage of the tapered line:

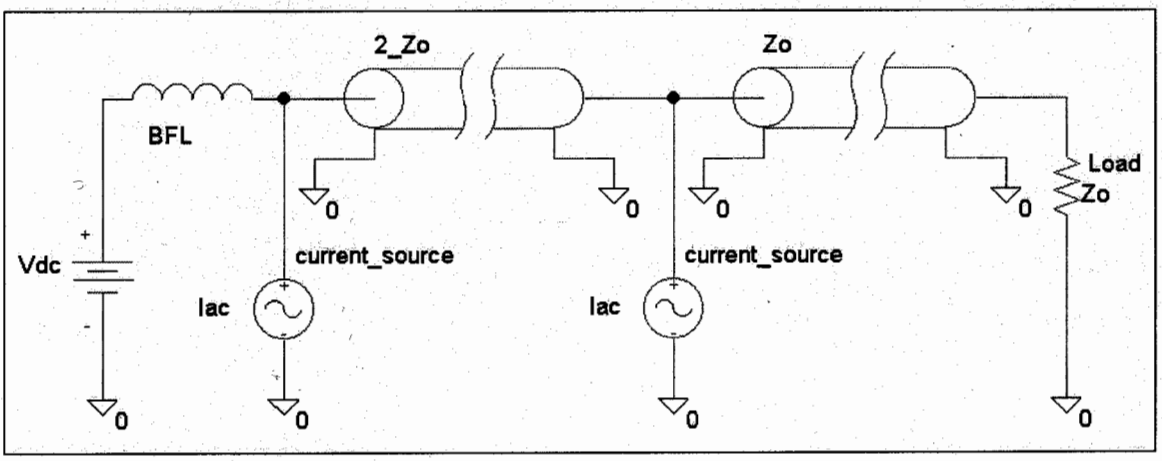


FIGURE 17.

A comparison of a tapered and non-tapered line has been made to emphasize the importance of tapering the line to avoid long transient regime. Our first tryout is shown in Fig 18. A generalized representation is shown in Figure 20 and the resultant load voltage for each case is shown in Figure 19.

Figure 18.

DISTRIBUTED AMPLIFIER

Tryout With Tapered Line Topology

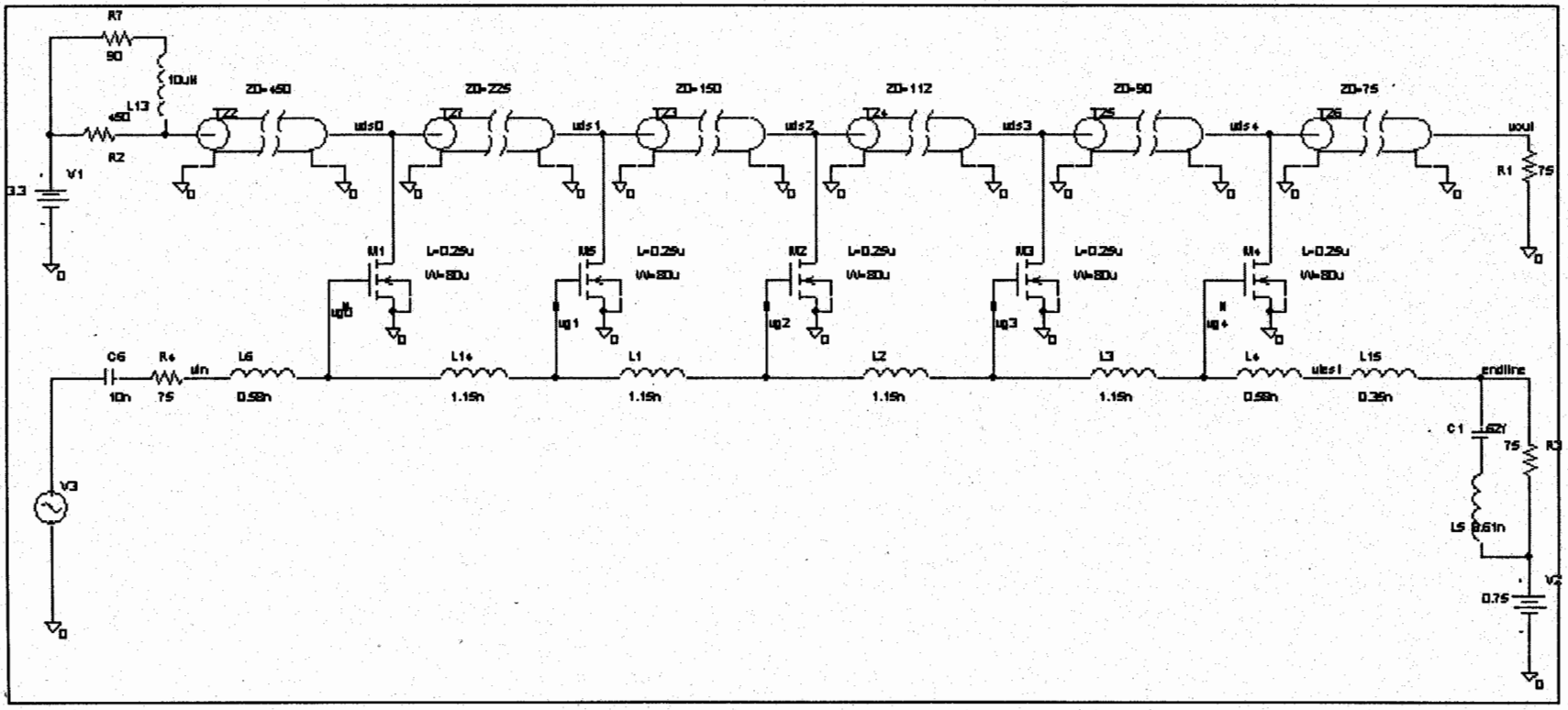
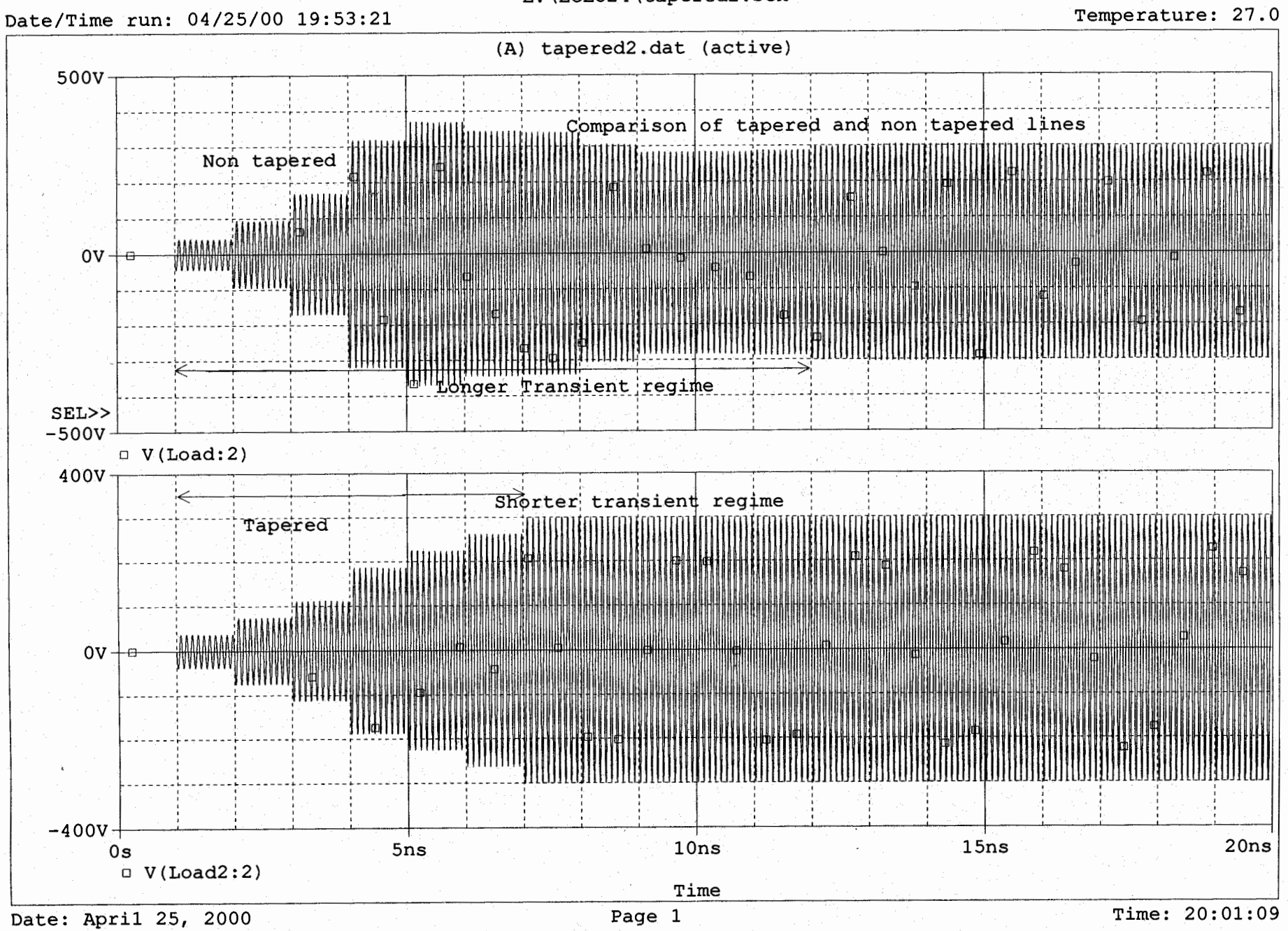


Figure 19. Transient response. Comparison of tapered vs. non-tapered drain lines.



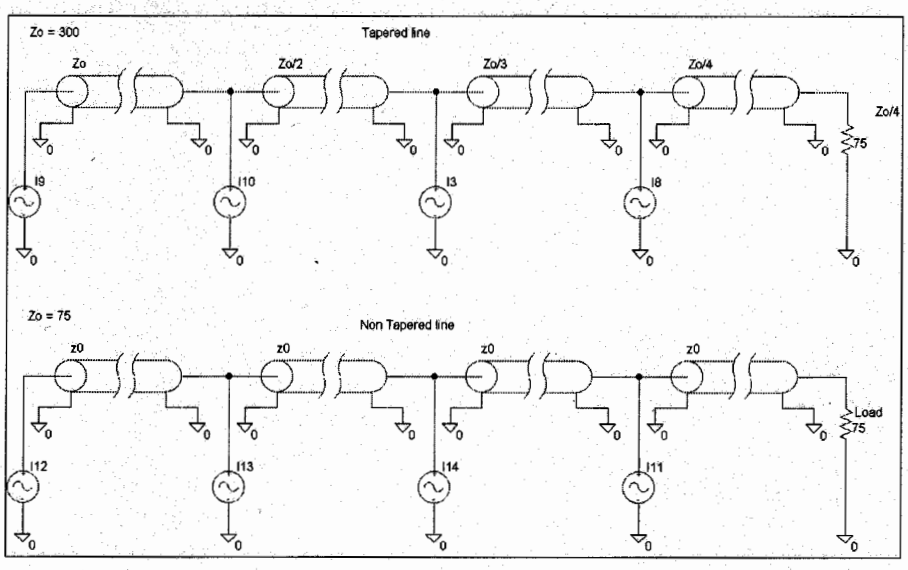


FIGURE 20.

b. The design issue of the tapered line

In order to design a tapered drain line, it is recommended to use different characteristic impedances along the line to avoid a long transient regime. This task is not an easy task and we ran into a design issue. Although the method to design the tapered transmission line is presented here, it was not employed in our final design.

Stated again, the main point is to design different characteristic impedances for each piece of the line.
To do so, the choice of the following two π -sections has been made.

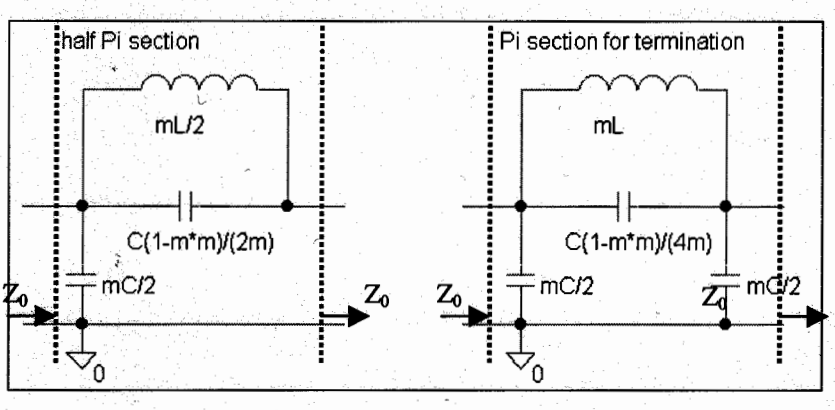


FIGURE 21.

For these sections, m has been chosen to equal 0.6.

The capacitance C is equal to $\frac{C_{eq,drain}}{2} + C_{extra}$.

Figure 22.

Π – Matching Sections as Pieces of Transmission Line

For Tapered line topology

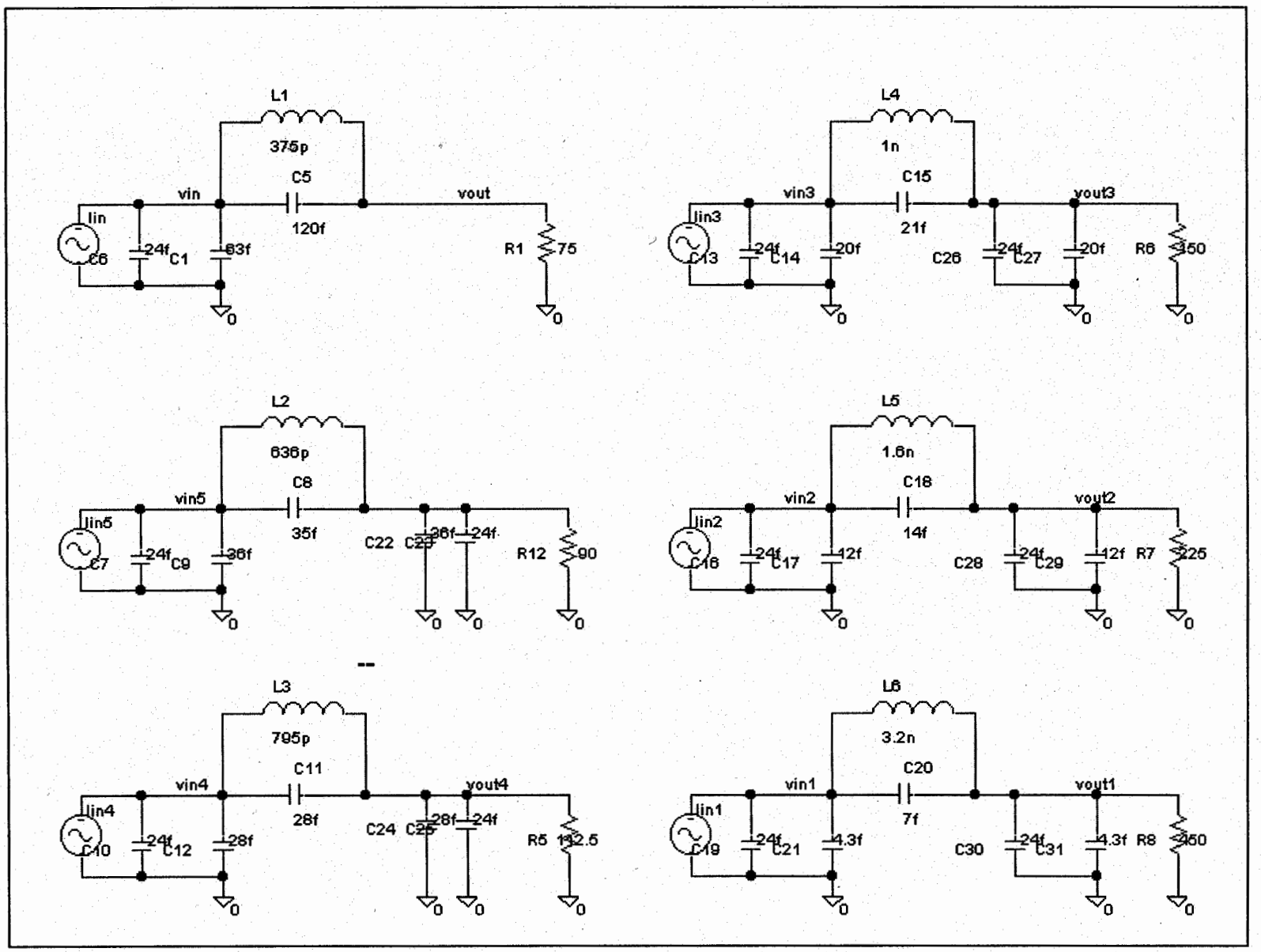
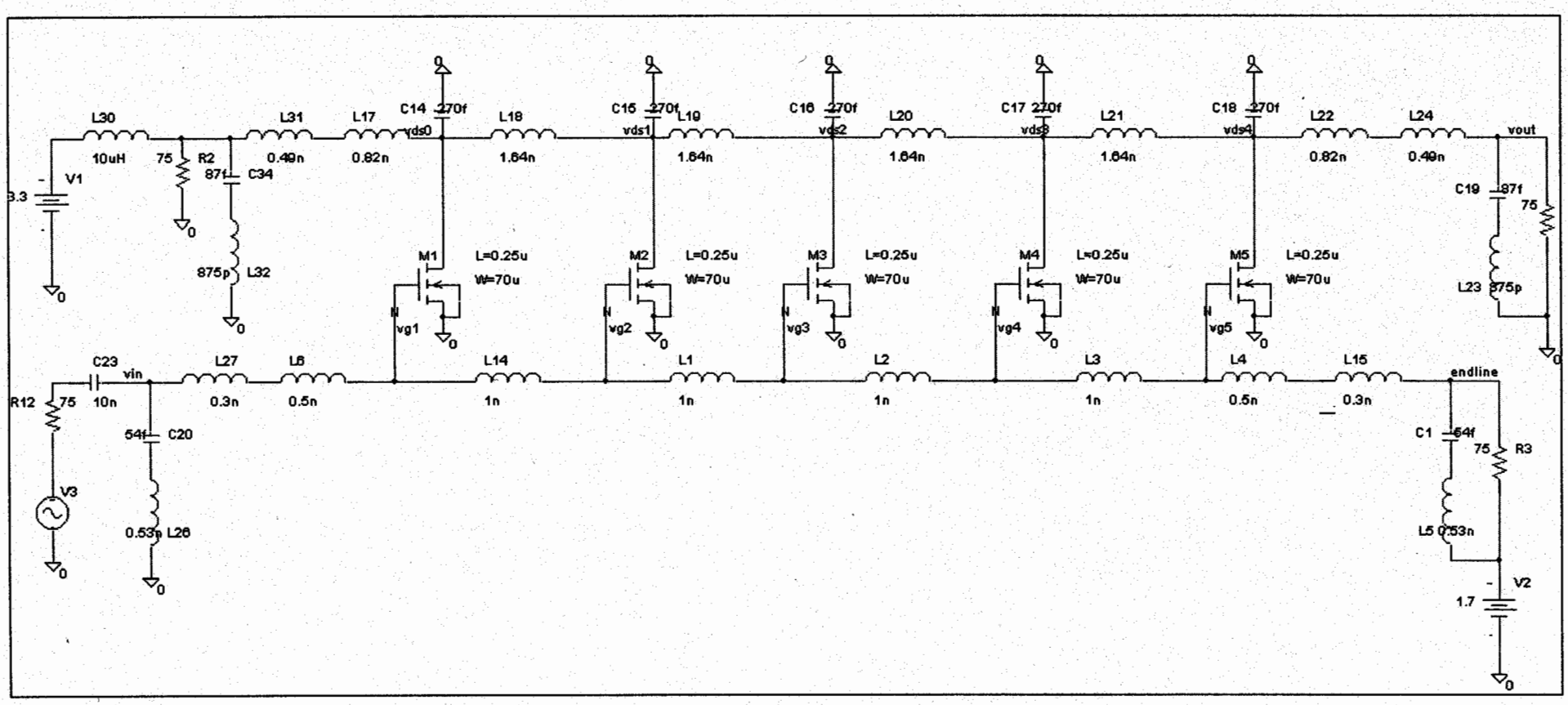


Figure 23. Second-to-last design

Design Before last without cascode stages

Drain Gate Feedback Issue



Each π -section has its own extra capacitance. The value of the inductance L must be found to satisfy the desired characteristic impedance and the corresponding time propagation delay.
The equations for the characteristic impedance and time delay are the following:

For a regular π -section:

$$C = \frac{\sqrt{2}t_d}{m * Z_0}$$

$$L = \frac{\sqrt{2}t_d Z_0}{m}$$

For a termination π -section:

$$C = \frac{2t_d}{m * Z_0}$$

$$L = \frac{2t_d Z_0}{m}$$

Once C is known, it is straightforward to obtain the value of the extra capacitance to use:

$$C_{extra} = C - \frac{C_{eq,drain}}{2}$$

The issue we encountered was the fact that each section should see different characteristic impedance, according to the tapered line principle. The problem is that if $\frac{Z_0}{n}$ is connected at the output of one section, then the image impedance seen from the input will be $\frac{Z_0}{n}$, whereas we would like to get $\frac{Z_0}{n-1}$.
We spent a lot a time trying to solve this issue, without success, and decided to use the non-tapered drain line. Nevertheless, we present our test circuits in Figure 22. Note in Fig. 22 the increasing value of the *Zo* load used to simulate the changing line impedance as one "sees" further down the tapered line.

D. Drain Gate Feedback Issue – Cascode stage

At this point, the *second-to-last* design revision is presented in Figure 23, and the need to use a cascode stages topology will now be justified.

a. Gate equivalent Capacitance variations

As already discussed, the equivalent gate capacitance $C_{eq,gate}$ is dependent on C_{gd} and the voltage gain A_v. For a narrow band application, A_v can be assumed constant. However, in the case of the distributed amplifier, the bandwidth is expected to be a few GHz wide. Thus, it is very likely that the gain will not exhibit perfectly flat behavior over the passband.

In theory, when the gate and drain lines do not have equal propagation delays, the expression for the gain becomes $A_v = \frac{-gm}{2\sqrt{1-\omega^2/\omega^2_{c,gate}}}\sqrt{\frac{L}{C}}\frac{\sinh[\frac{N(\theta_g-\theta_d)}{2}]}{\sinh[\frac{(\theta_g-\theta_d)}{2}]}e^{-N(\theta_g+\theta_d)}$ where,

$\omega_{c,gate}$ = cutoff frequency of the gate transmission lines (assumed equal).

θ_g, θ_d = propagation constant of the gate and drain transmission line.

Unlike our earlier expression for gain, the extra sinh ratio term here causes a decrease in the voltage gain. A plot of this extra term is given in Figure 24.

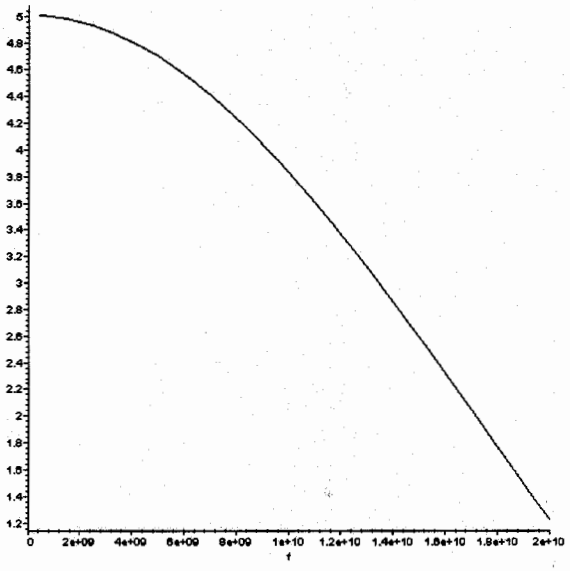


FIGURE 24. -- sinh ratio vs. frequency

The plot of the voltage gain for this *second-to-last* revision of our distributed amplifier is given in Figure 25, and a plot of the equivalent capacitance seen from the gate of one transistor is given in Figure 26. From these plots, note the bad variations in voltage gain make the $C_{eq,gate}$ vary in a strong fashion.

b. The cascode solution

To alleviate this feedback effect, one can employ a cascode topology, as shown in Figure 27.

Figure 25. Variation in voltage gain (Second-to-last design)

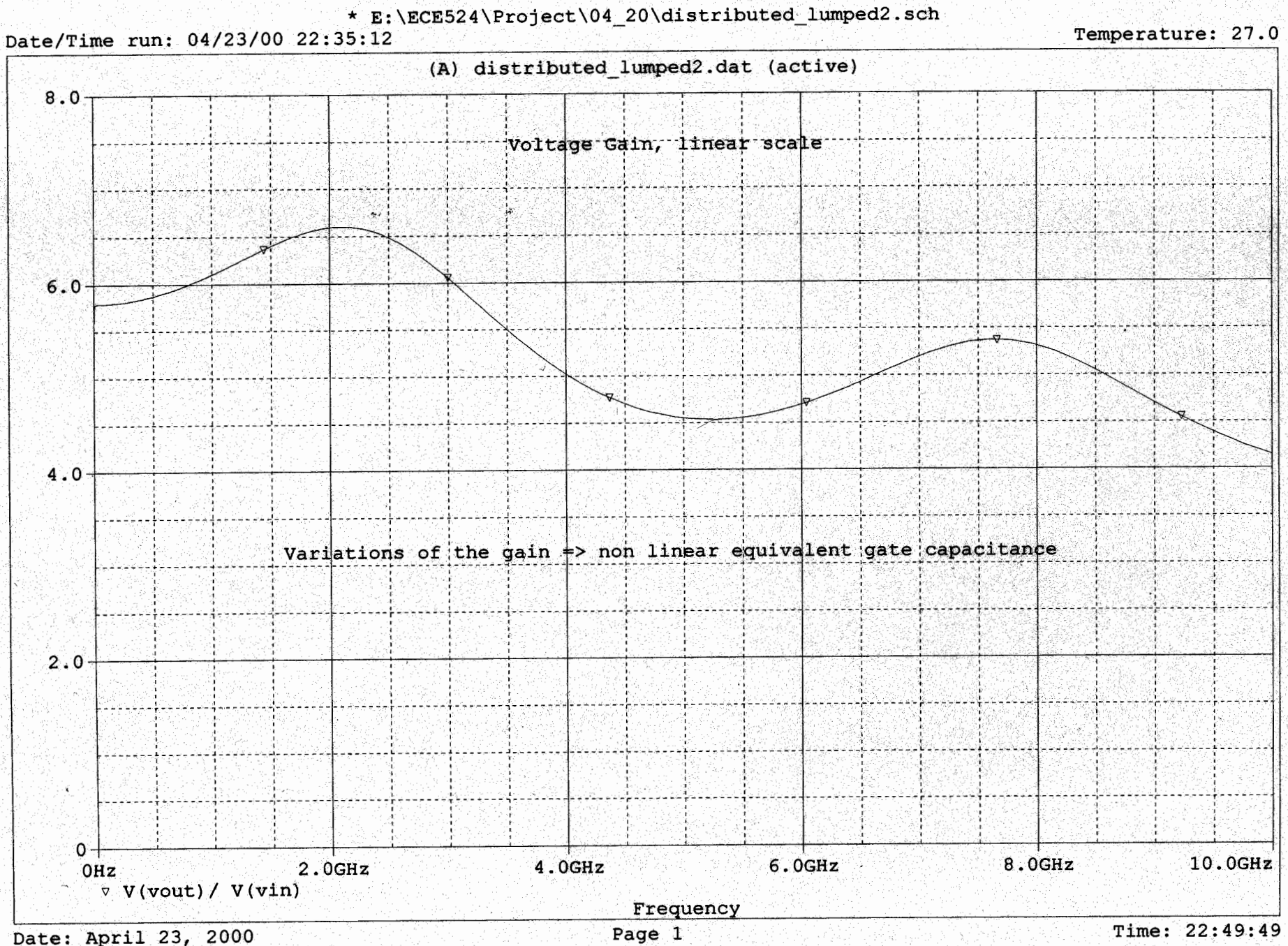
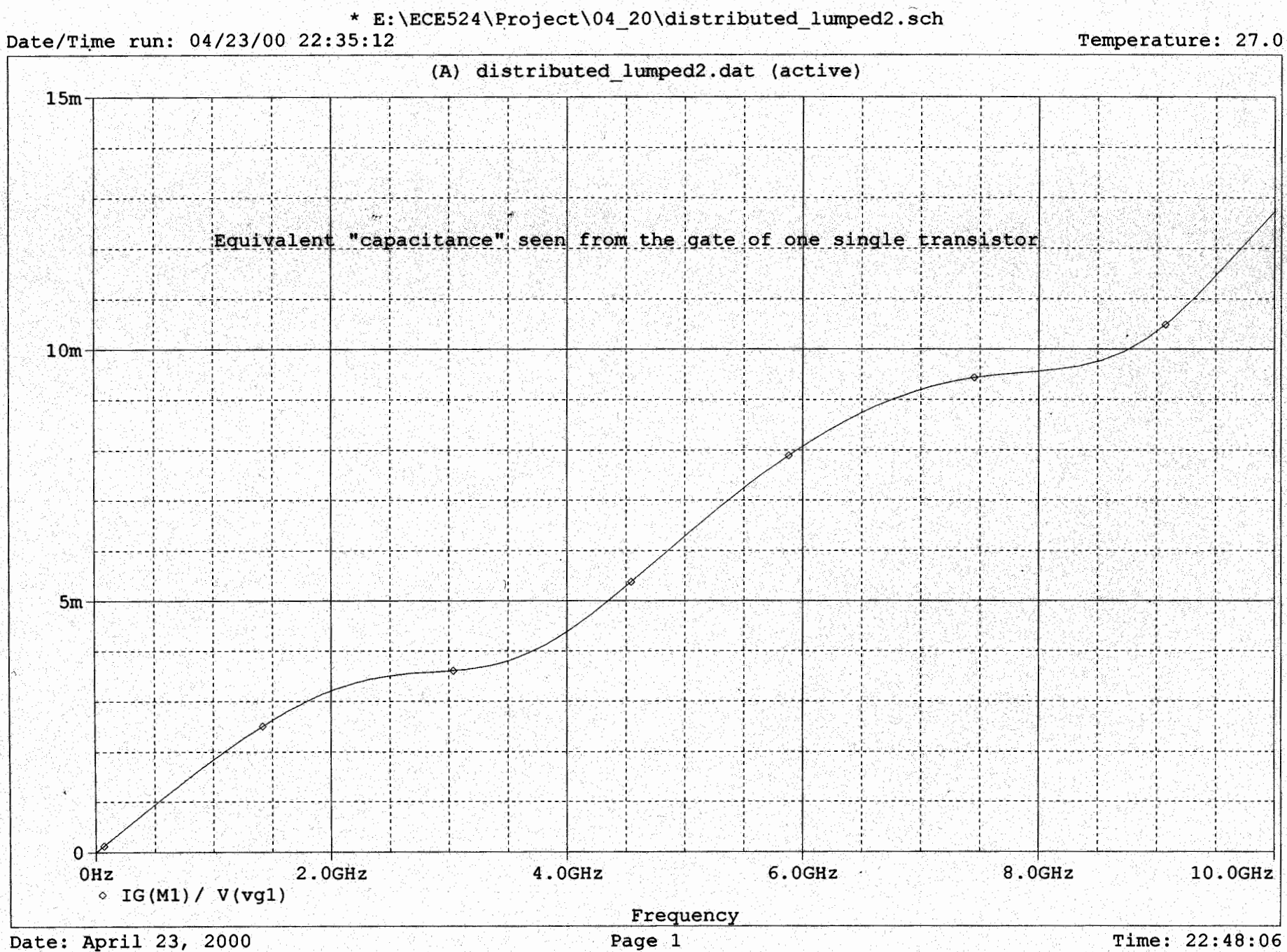


Figure 26. Variation in capacitance seen by gate of one single transistor (Second-to-last design)



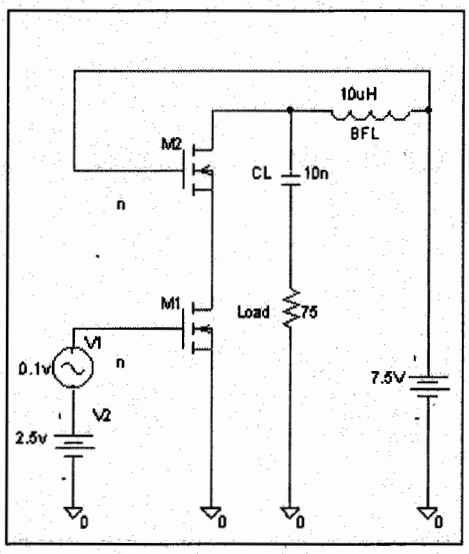


FIGURE 27. One cascode stage extracted from the schematic

To derive the new equivalent capacitance seen from the gate, the small signal model is needed.
This small signal model of the cascode stage is shown in Figure 28:

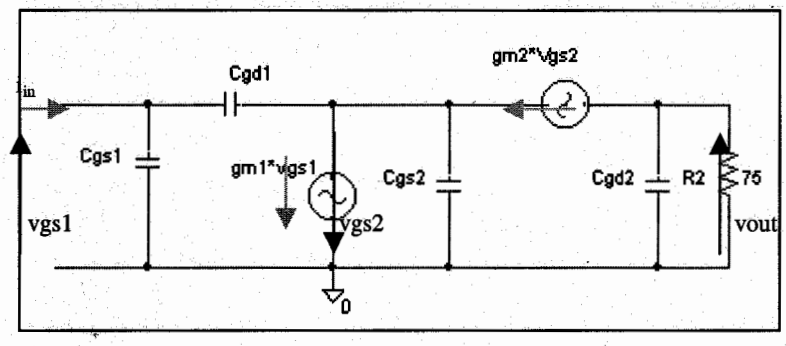


FIGURE 28.

The input admittance is given by $\frac{i_{in}}{v_{gs1}} = C_{gs1}s + C_{gd1}s + C_{gd1}s\frac{g_{m1}}{g_{m2}}\left(\frac{1-\frac{C_{gd1}s}{g_{m1}}}{1+s(\frac{C_{gd1}+C_{gs2}}{g_{m2}})}\right)$.

We can easily note that $\frac{i_{in}}{v_{gs1}} \approx C_{gs1}s + C_{gd1}s(1+\frac{g_{m1}}{g_{m2}})$.

Therefore, the equivalent capacitance seen from the gate of the cascode stage is:

$$C_{gate,cascode} = C_{gs1} + C_{gd1}(1+\frac{g_{m1}}{g_{m2}}) .$$

This new capacitance is now constant and the non-linear capacitance effect seen before is avoided.

The equivalent capacitance seen from the drain end (i.e., the drain transmission line) is simply:

$C_{eq,drain} = C_{gd2}$

The voltage gain of the overall stage is given by $A_v \approx -g_{m1} * R_{load}$, because the stage including M2 has a voltage gain of approximately 1. Therefore, hardly any change in the overall voltage gain of the distributed amplifier will be seen when cascode stages are used.

c. The voltage issue

Cascode stages are a good idea, but both M1 and M2 transistors need to be in saturation for proper operation. To ensure this, the gate of M2 has been tied to the DC supply voltage to ensure proper turn on of M2. In getting both transistors in saturation, the strategy was to maximize the transconductance of M1, since the voltage gain is driven by g_{m1}. *The issue was that we could not get the two transistors in saturation with only a 3.3V DC supply voltage.* So, the DC voltage was doubled -- the actual bias used is Vgs_{M2} = 3V and Vgs_{M1} = 2.5V, yielding drain Vds voltages of 4.5V and 3V for M1 and M2, respectively.

The characteristic plot of the transistor shown in Figure 29 proves that we are operating in saturation. (The bias of the gate line was swept until the maximum AC g_{m1} was reached and an optimal value of 37mS became available. See Figure 30).

d. Final topology

Thus, by using a cascode topology – as shown in our final, main schematic in Figure 31 -- the gain in the passband is given by $|A_v| \approx \frac{-N * gm}{2}\sqrt{\frac{L}{C}} = 6.9$. This value is precisely that which is observed in Figure 31, where the gain of the cascode distributed amplifier is plotted.

E. A note on transistor dimensions – Choosing W and L

Initially, a 4-stage distributed amplifier topology was chosen, with each transistor having W = 100u. This large value of W resulted in low bandwidth (due to the width dependent C_{gs}), and low output power.
A value of W = 80u helped the gain, but bandwidth still suffered due to the high C_{gs}.
Finally, it was found that at W =70u, good bandwidth could be obtained. However, due to the lower gain of each transistor at W = 70u (lower gm), a fifth stage was added, resulting in good gain too !

Figure 29. Transistor characteristic curves (final design)

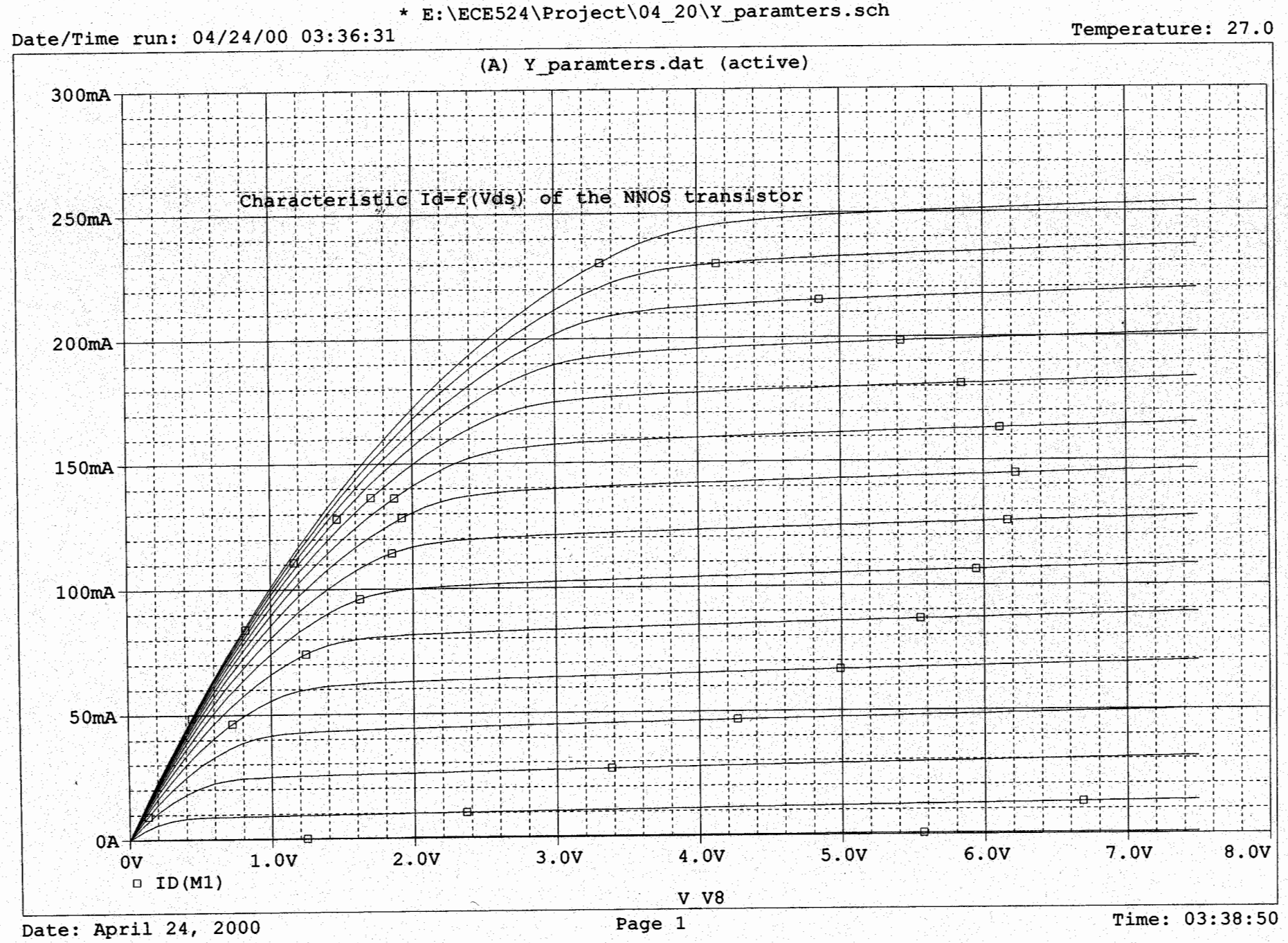


Figure 30. choosing the optimal gm (final design – cascode topology)

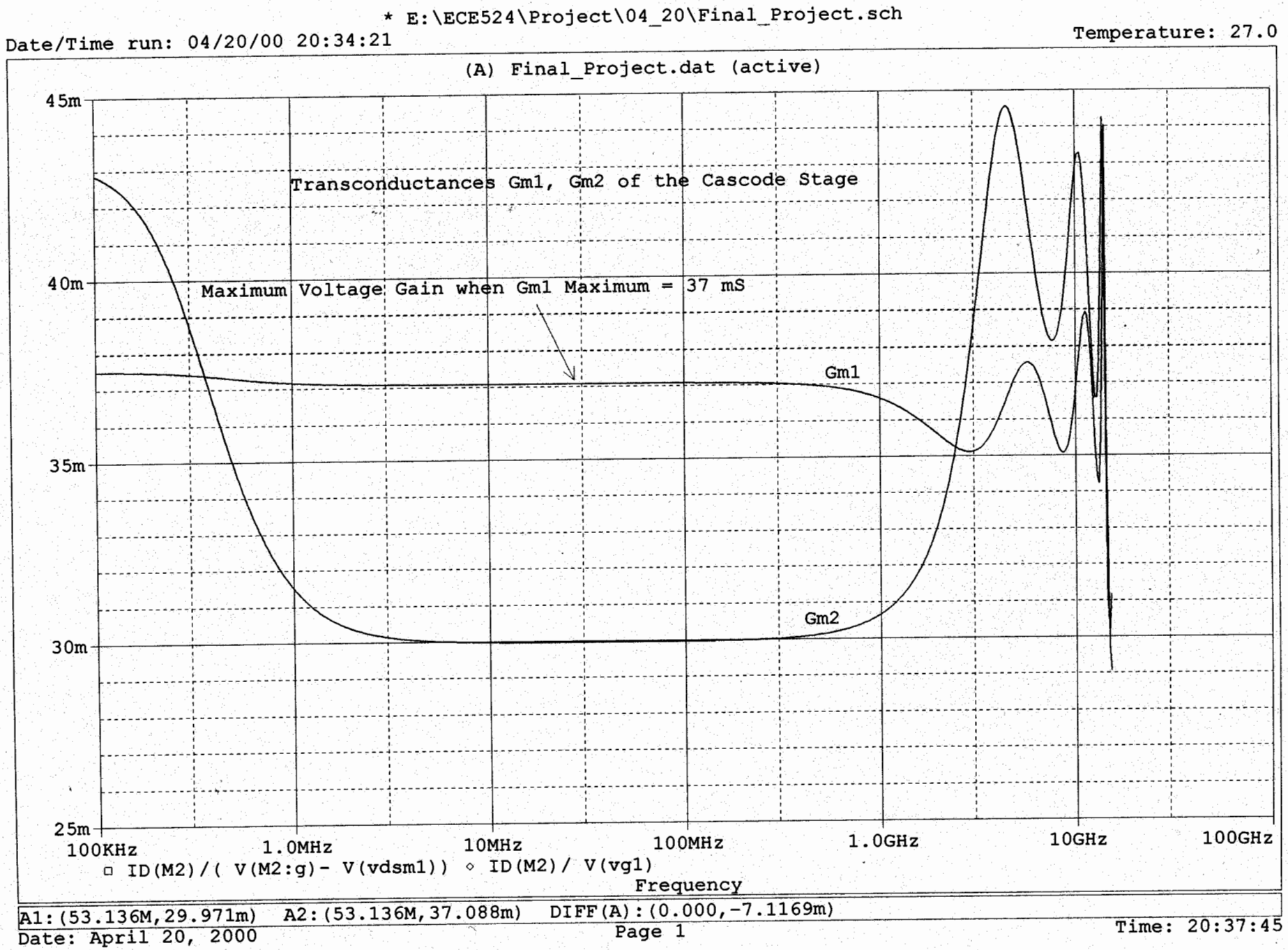
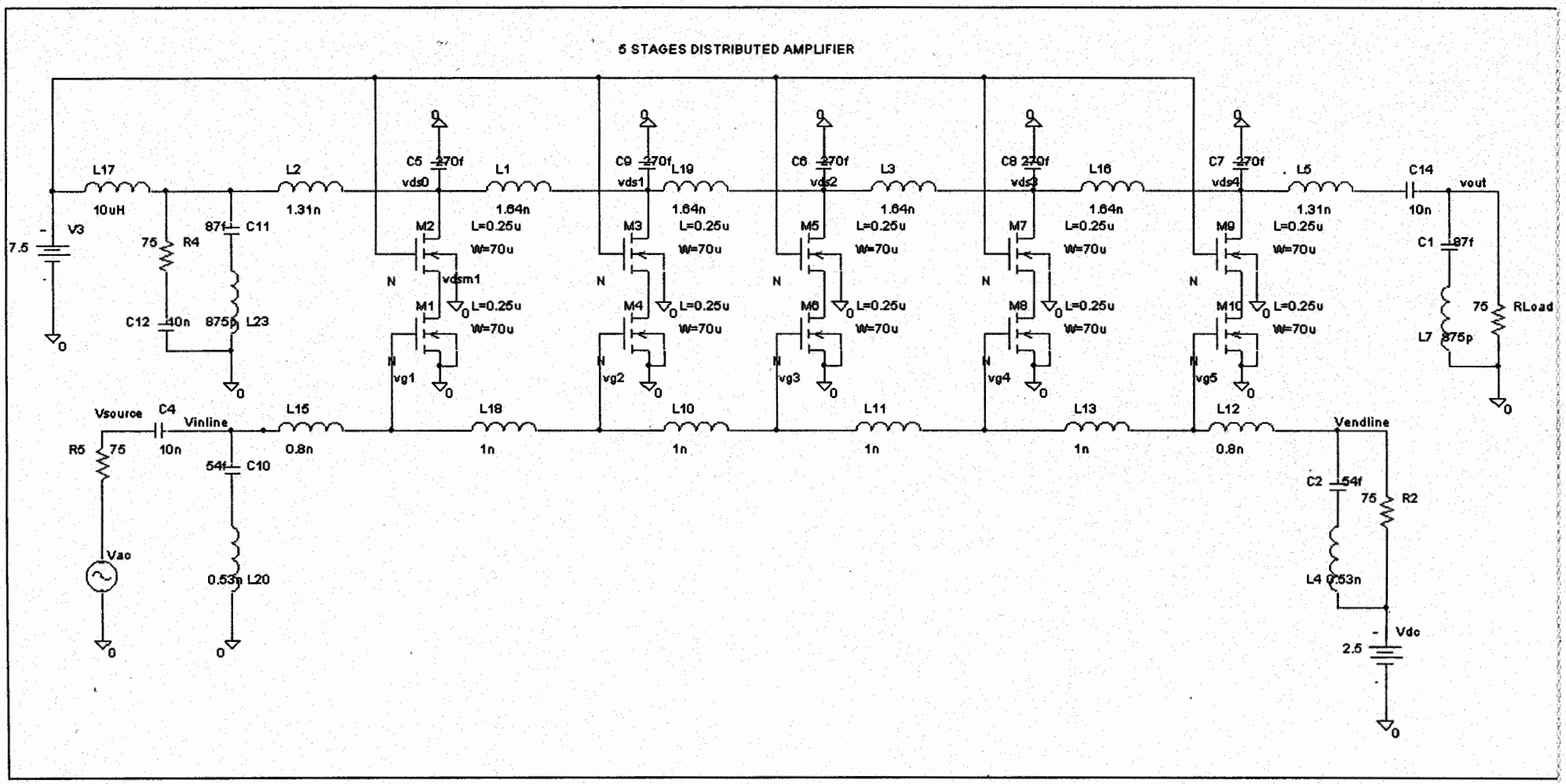


Figure 31.

5 STAGES DISTRIBUTED AMPLIFIER

MAIN SCHEMATIC



PART III : RESULTS

A. Design Requirements

We started with these working specification for our distributed amplifier:

1. .5 to 5.0 GHz
2. 2. 5 dB gain
3. 3. 1 milliwatt RF output power*
4. Zo = 75 Ω

(CATV impedances are 75 Ω because this value approximately corresponds to minimum loss.)

*The standard for power measurement is the dBmV (decibels referenced to 1 millivolt across 75 Ω)

B. Derived topology

See Figure 31 – Main Schematic

C. Measurements vs. requirements

Using the derived topology of Figure 31, a good agreement is observed between the attached measurement plots, and our specifications:

FIGURE 32 Gain vs. Frequency (linear scale)
FIGURE 33 Gain vs. frequency (dB scale)

FIGURE 34 Power in a 75 Ω load (at 1 dB compression) vs. frequency
FIGURE 35 Rms output power

FIGURE 36 Real & Imaginary input impedance vs. frequency

FIGURE 37 Time delay between stages

FIGURE 38 Vout/Vin phase response – frequency domain
FIGURE 39 Vout/Vin phase response -- time domain

PART IV : CONCLUSION

We have shown the distributed amplifier to be highly effective when wide bandwidth is desired, without an accompanying loss of gain.

Studying the theory and simulation of a distributed amplifier will entail a confluence of your knowledge of circuit, transmission line and wave theories. In doing so, you can utilize your experience with these theories, but please leave behind any preconceived notions of what can and can not be done!

Figure 32. Gain vs. Frequency (linear scale)

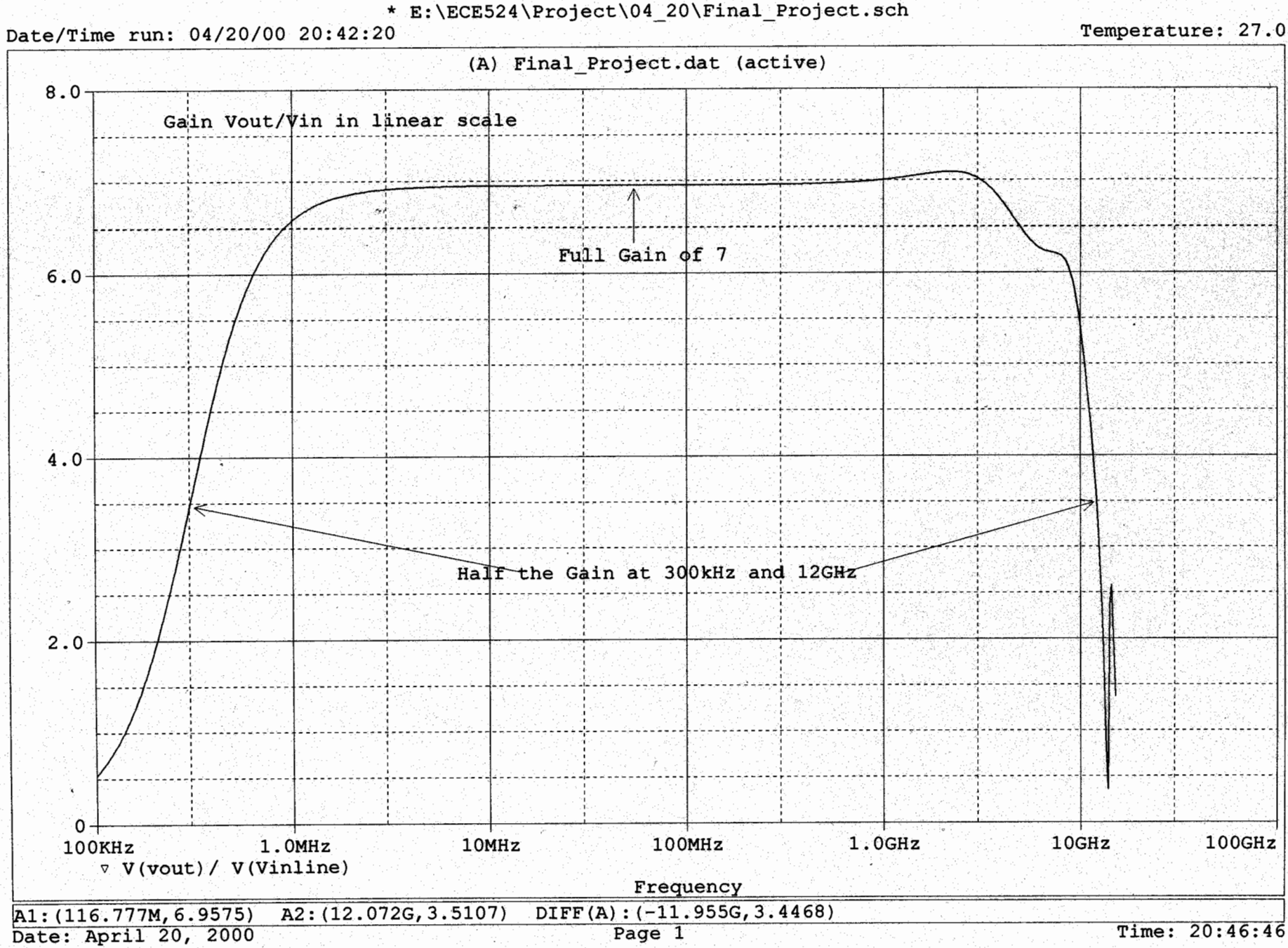


Figure 33. Gain vs. Frequency (dB scale)

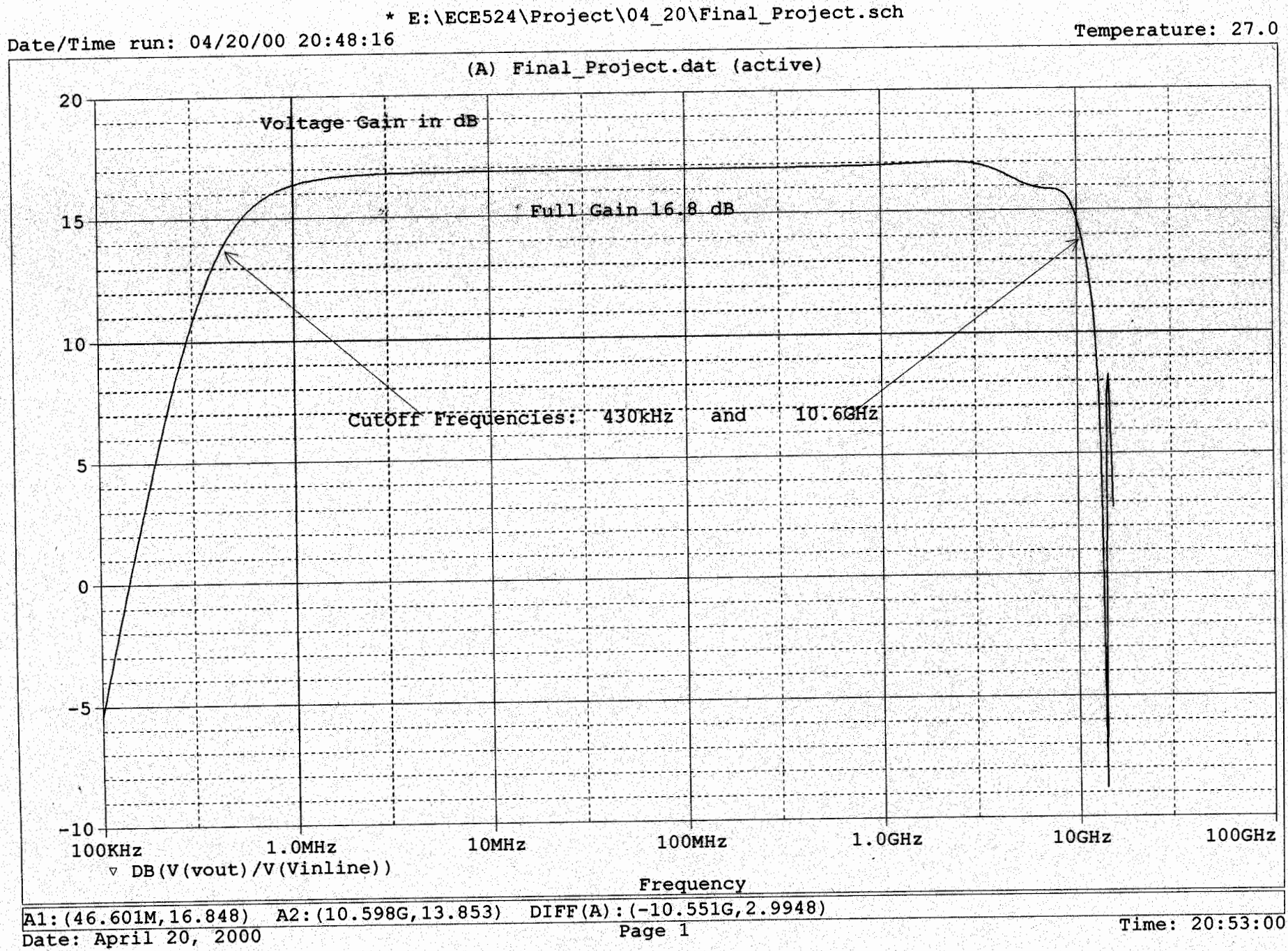


Figure 34. Power in a 75 Ω load (at 1 dB compression) vs. frequency

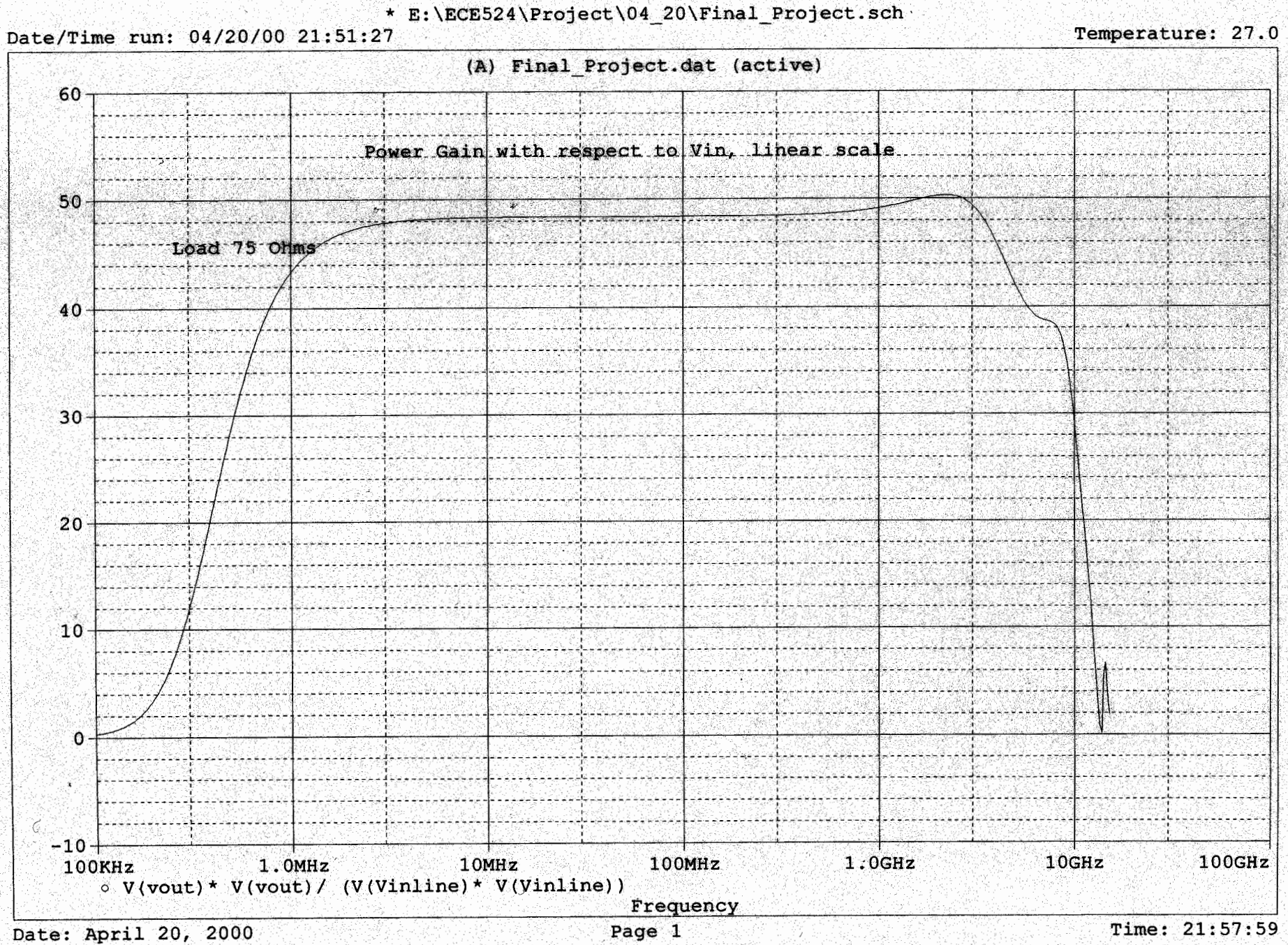


Figure 35. Rms output power

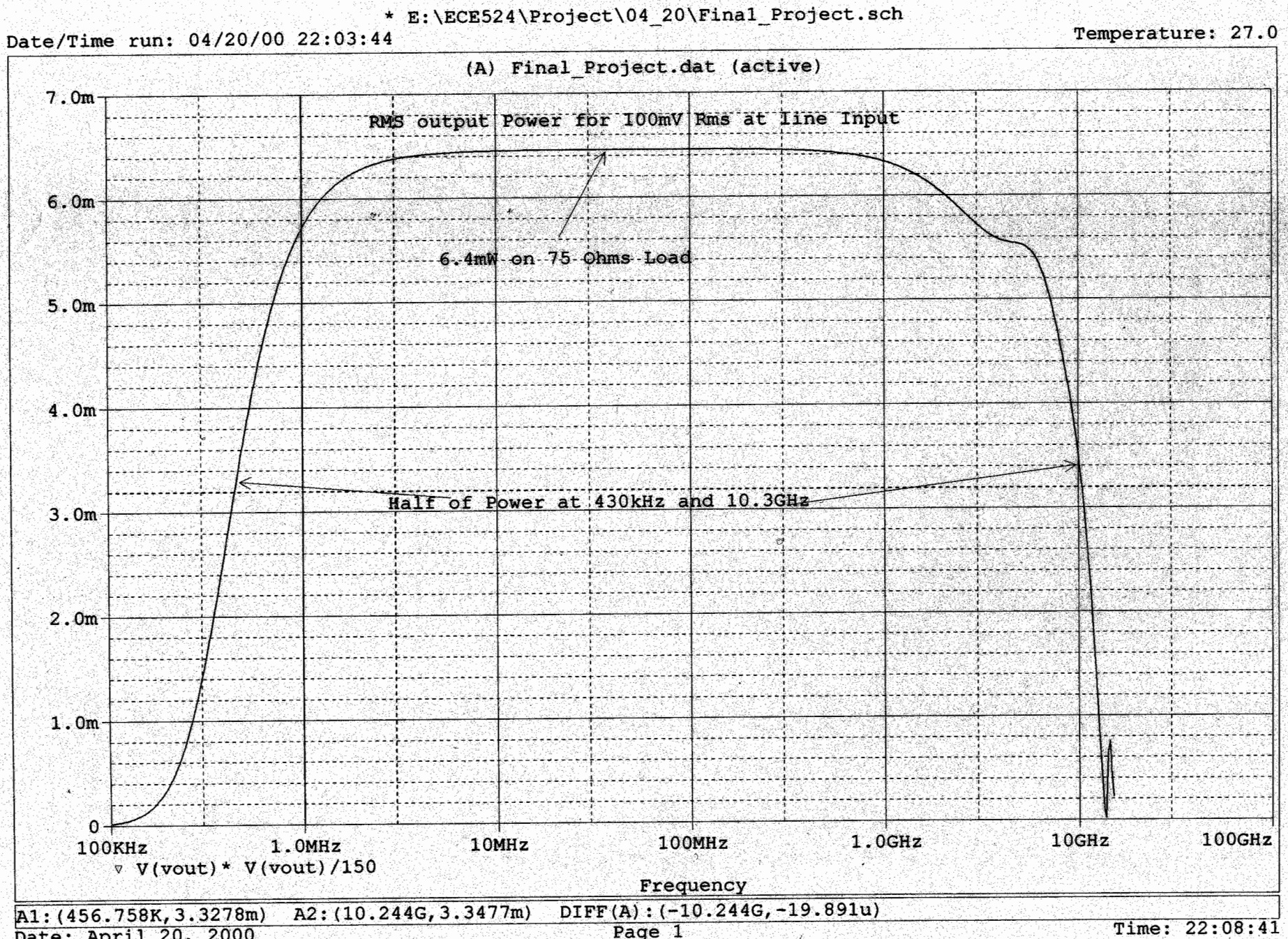


Figure 36. Real and Imaginary input imdeances vs. frequency

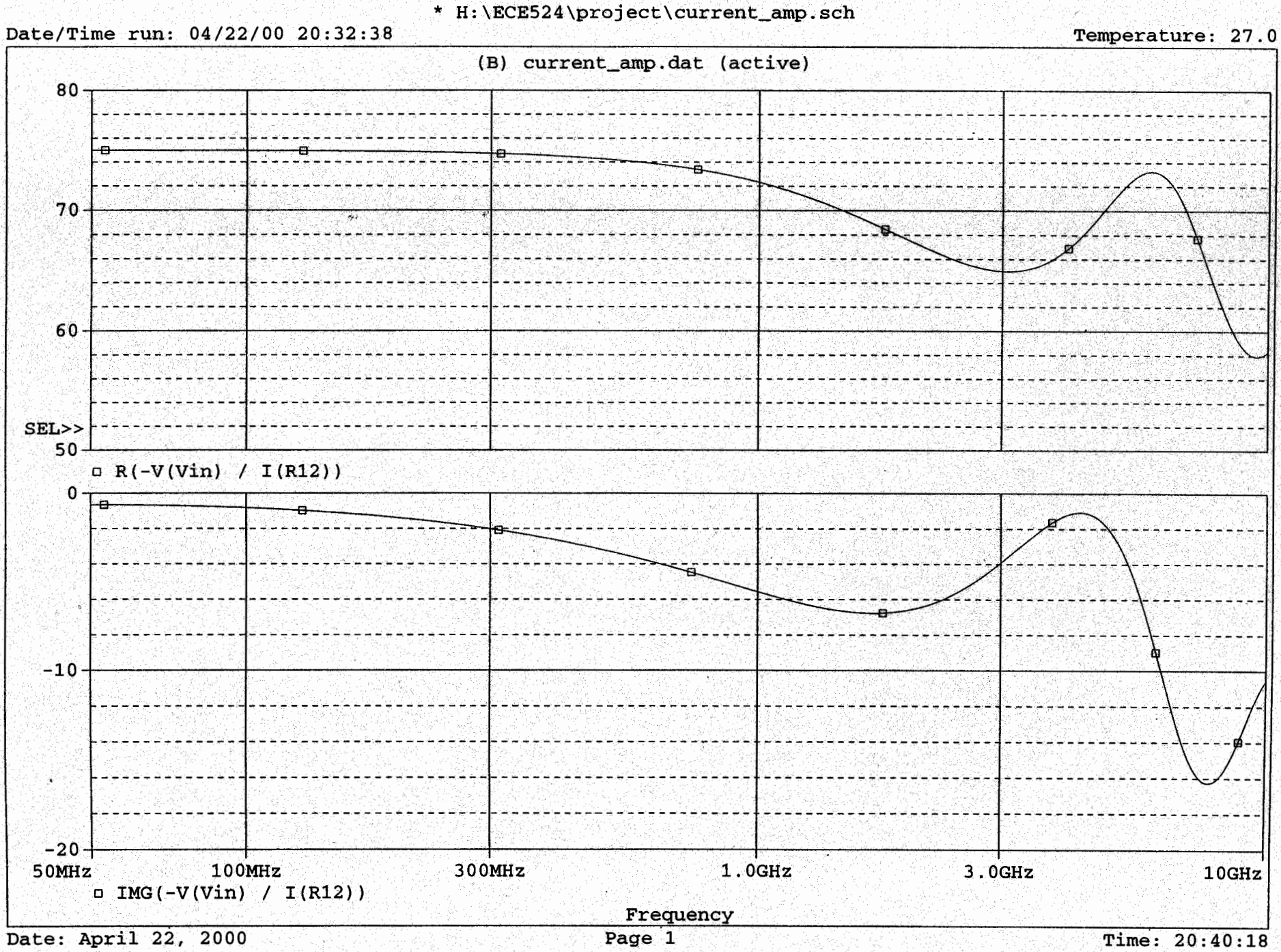


Figure 37. Time delay between stages

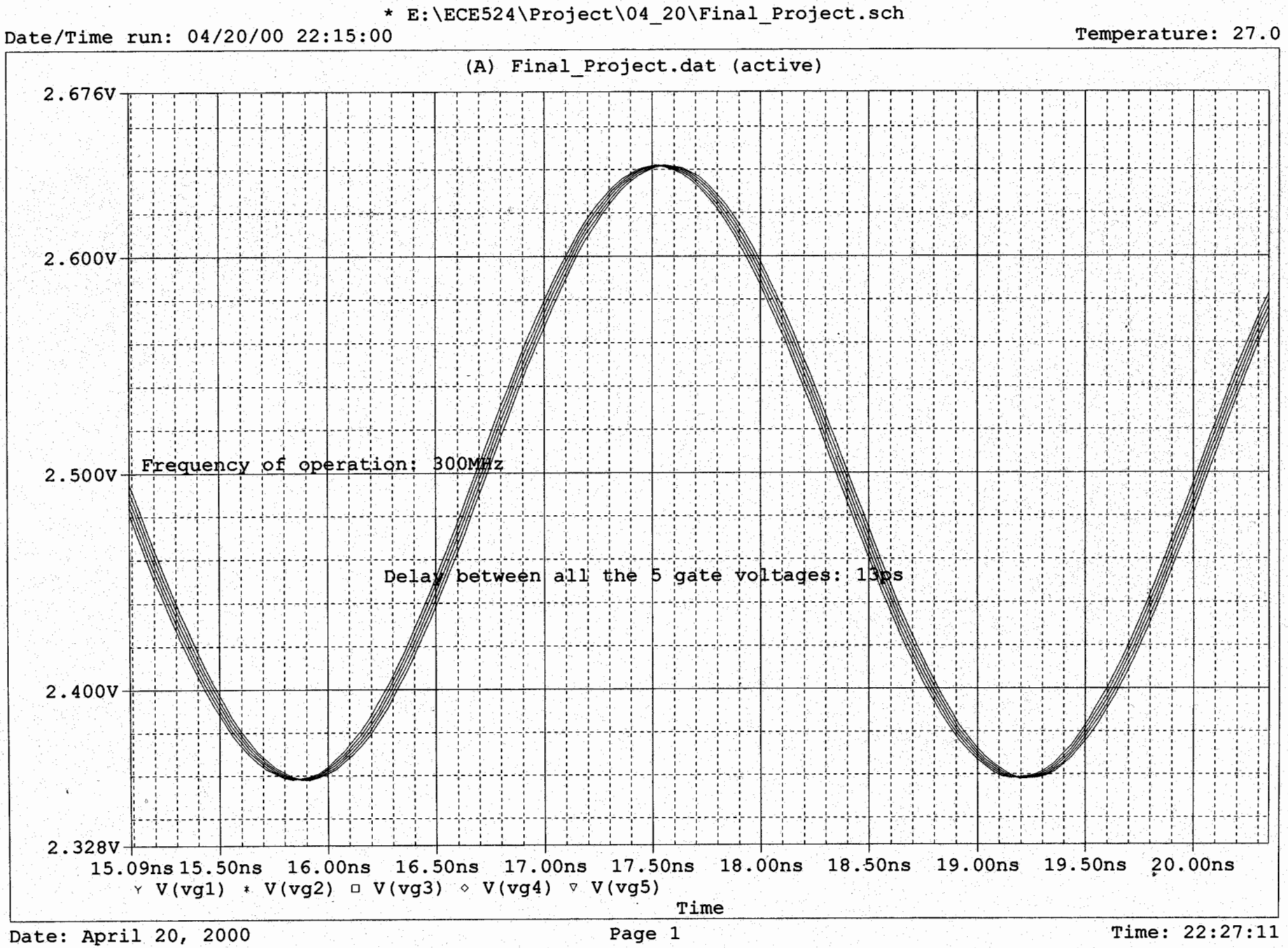


Figure 38. Phase response – frequency domain

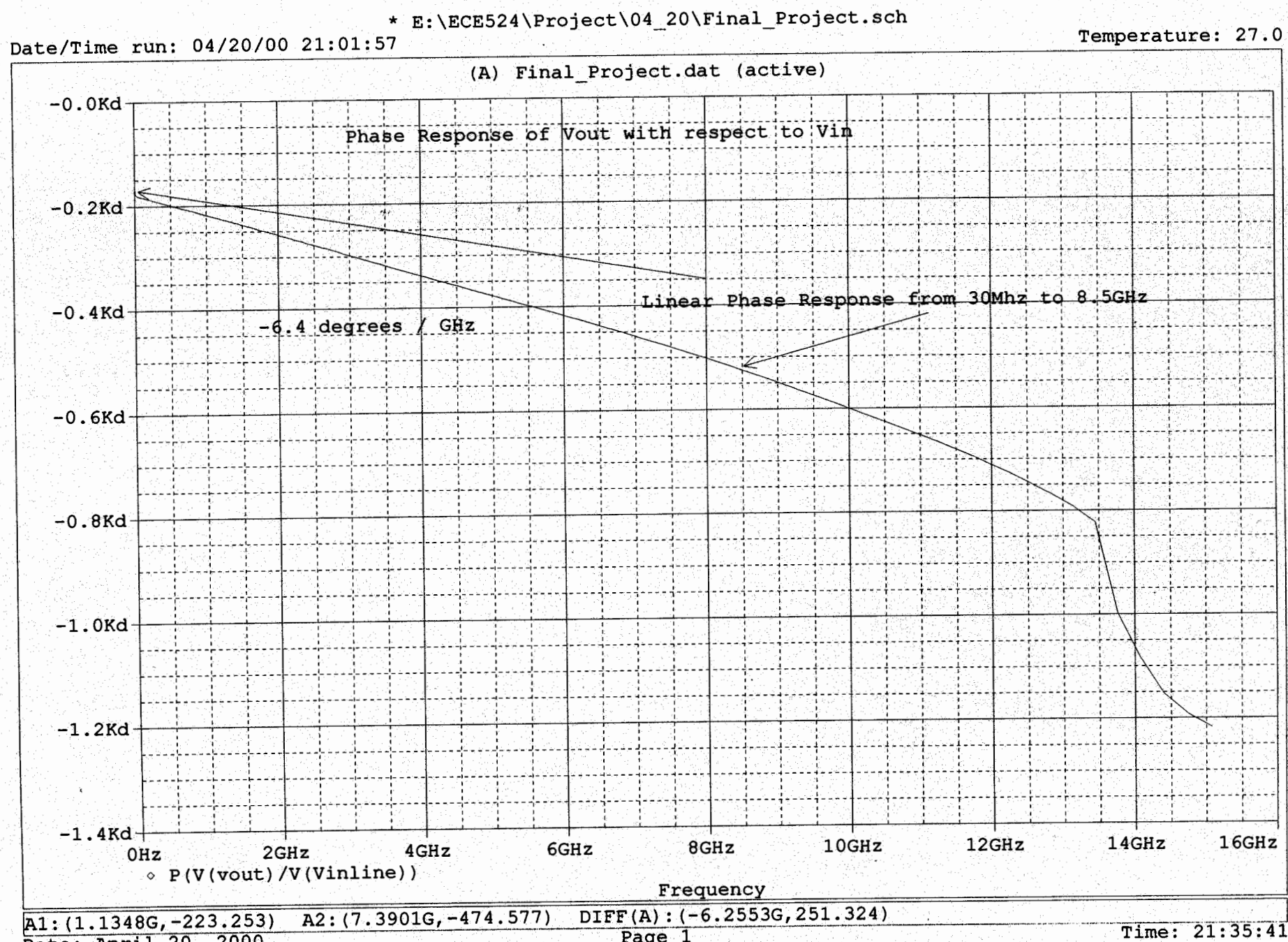
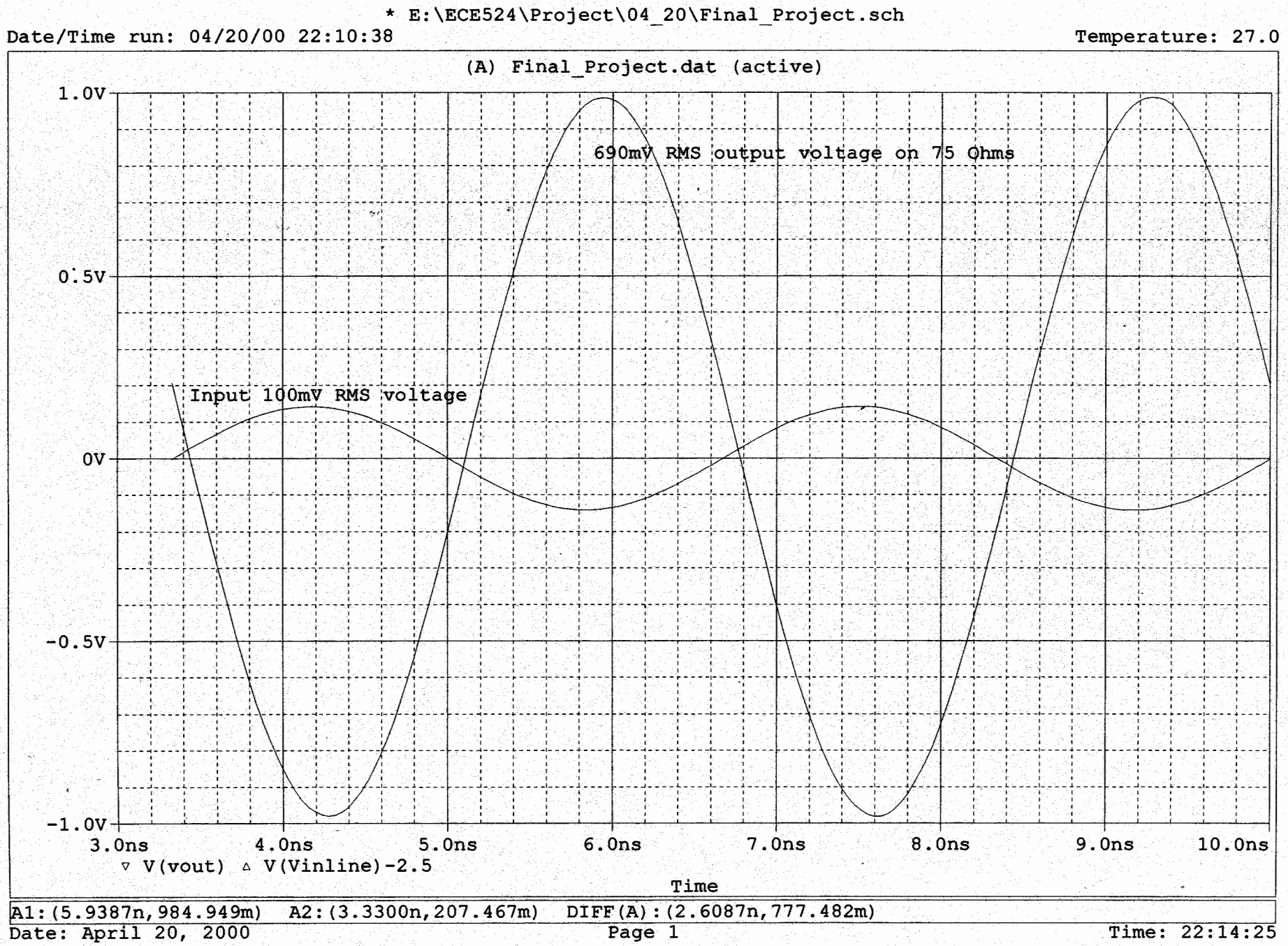


Figure 39. Phase response – time domain



PART V : REFERENCES

(1) T.H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, chapters 5,8, Cambridge U. Press, 1998.

(2) B. Ballweber, R. Gupta, D. Allstot, "A Fully Integrated 0.5-5.5-GHz CMOS Distributed Amplifier," IEEE Transactions on Solid-State Circuits, vol. 35, No. 2, pp. 231-239, February 2000.

(3) T. Wong, *Fundamentals of Distributed Amplification*, chapters 1,2,3,4,6, Artech House, 1993.

(4) G. Vendelin, A. Pavio, U. Rohde, *Microwave Circuit Design Using Linear and Nonlinear techniques*, chapter 5, John Wiley & Sons , Inc., 1990.