ECE 587 – Hardware/Software Co-Design
Spring 2019

Instructor: Professor Jia Wang
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Prerequisite:
CS 201 Introductory data structures, algorithms, and object-oriented programming.
ECE 441 Microprocessors, memories, I/O interfaces, and interrupt systems.

Though not required, you are recommended to take at least one course among ECE 429, ECE 449, and ECE 485 before taking this course.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Tue./Thur.: 5:00 PM – 6:15 PM
Class Location: Perlstein Hall 131
Class Home Page: `http://www.ece.iit.edu/~jwang/ece587-2019s/`

Office Hrs: Tue./Thur.: 3:30 PM – 4:30 PM

Recommended Textbook: "Embedded System Design: Modeling, Synthesis and Verification"
D. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Springer, 2009.
ISBN-13: 978-1-4419-0503-1 (eBook available from `http://library.iit.edu/`)

Course Objective: To give students a clear understanding of state-of-the-art hardware/software co-design methodology for computing systems.

Topics Covered: Hardware/software co-design of computing systems; Models of computation and functional verification; Transaction-level modeling and performance evaluation; high-level synthesis and hardware acceleration.

Grading: Homeworks: 25% / Project: 75%.
A: $\geq$ 90% / B: $\geq$ 80% / C: $\geq$ 60%.

Teaching Assistants: TBD

Homework and Project Policy: Late homeworks and projects will not be graded. Deadlines will NOT be extended, except for extraordinary reasons. Homeworks will be graded based on general approach and completion, and solutions will be released shortly after due date. Discussions on homeworks/projects are encouraged, but copying will call for disciplinary action.

Lecture Schedule (tentative):

No.	Date	Topic	HW
1	1/15, 1/17	Introduction	
2	1/22, 1/24	Models of Computation I	
3	1/29, 1/31	Models of Computation II	HW #1
4	2/5, 2/7	Models of Computation III	
5	2/12, 2/14	Models of Computation IV	HW #2
6	2/19, 2/21	Verification	
7	2/26, 2/28	Transaction-Level Modeling I	
8	3/5, 3/7	Transaction-Level Modeling II	HW #3
9	3/12, 3/14	System Design Methodology	
10	~~3/19~~, ~~3/21~~	**Spring Break**	
11	3/26, 3/28	Software Synthesis	
12	4/2, 4/4	Hardware Synthesis	HW #4
13	4/9, 4/11	Hardware Acceleration I	
14	4/16, 4/18	Hardware Acceleration II	
15	4/23, 4/25	Hardware Acceleration III	
16	4/30, 5/2	Hardware Acceleration IV	