1. (30 points) Consider the following sequential program that should be implemented as a hardware component.

inputs/outputs: B,C,D,X,Y  
temporary variables: A,E

\[
\begin{align*}
A &= B + C \times 3; \\
B &= B + C + D; \\
E &= A \times A; \\
X &= C + D + Y; \\
D &= A + E;
\end{align*}
\]

Assume there are one 2-input multiplier, which can generate a result in 4 clock cycles, and two 2-input adders, which can generate a result in 2 clock cycles. Follow the simplified HLS design flow introduced in Lecture 20 and 21 to

1) Decide the scheduling and binding of functional units  
2) Allocate and bind storage units  
3) Design FSMs for the control unit