1. (30 points) Consider the following sequential program that should be implemented as a hardware component.

inputs/outputs: B,C,D,X,Y
temporary variables: A,E

A=B+C*3;
B=B+C+D;
E=A*A;
X=C+D+Y;
D=A+E;

Assume there are one 2-input multiplier, which can generate a result in 4 clock cycles, and two 2-input adders, which can generate a result in 2 clock cycles. Follow the simplified HLS design flow introduced in Lecture 19 and 20 to

1) Decide the scheduling and binding of functional units
2) Allocate and bind storage units
3) Design FSMs for the control unit

Answer:

The dataflow graph is shown in the following figure. Note two variables u1 and u2 are introduced since we assume adders only add two numbers at a time.
We need 12 control steps as shown below.

We need 5 registers for B, C, D, X, Y, and 2 registers for u1, u2, A, E.
Consider the control signal for R1 and R2. The corresponding FSMs are defined in the following table.

<table>
<thead>
<tr>
<th>Port</th>
<th>csteps</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>R1</td>
<td>*</td>
</tr>
<tr>
<td>R2</td>
<td>*</td>
</tr>
</tbody>
</table>