ECE 587 – Hardware/Software Co-Design
Fall 2012

Instructor: Professor Jia Wang
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Prerequisite:
CS 201 Introductory data structures, algorithms, and object-oriented programming.
ECE 441 Microprocessors, memories, I/O interfaces, and interrupt systems.

Though not required, you are recommended to take at least one course among ECE 429, ECE 449, and ECE 485 before taking this course.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Tue./Thur. 10:00 AM – 11:15 AM
Class Location: Engineering 1, Room 244
Class Home Page: `http://blackboard.iit.edu/`

Office Hrs: TBD

Required Textbook: "Embedded System Design: Modeling, Synthesis and Verification"
D. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Springer, 2009. ISBN-13: 978-1-4419-0503-1

Course Objective: To give students a clear understanding of modern embedded system design methodologies.

Topics Covered: Hardware/software co-design of embedded systems; models of computation; transaction-level modeling; processor and communication modeling; task and communication synthesis; high-level synthesis; design optimization; verification.

Grading: Homeworks: 10% / Projects: 40% / Midterm Exam: 20% / Final Exam: 30%.
A: $\geq$ 90% / B: $\geq$ 75% / C: $\geq$ 60%.

Teaching Assistants: TBD

Homework and Project Policy: Late homeworks and projects will not be graded. Discussions on homeworks/projects are encouraged, but copying will call for disciplinary action.

Exam Policy: Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

No.	Date	Topic	Chapters	HW & Project
1	8/21, 8/23	Introduction	1,2	
2	8/28, 8/30	State-Based Models	3.1	
3	9/4, 9/6	Process-Based Models	3.1	HW #1
4	9/11, 9/13	SystemC	3.2, Notes	PRJ #1
5	9/18, 9/20	System Modeling	3.3	
6	9/25, 9/27	Processor and Communication Modeling	3.4, 3.5	
7	10/2, 10/4	Transaction-Level Models	3.6, Notes	
8	10/9, 10/11	Midterm Exam Review, **Midterm Exam**		PRJ #2
9	10/16, 10/18	System Synthesis	4	
10	10/23, 10/25	Task Synthesis	5	HW #2
11	10/30, 11/1	Communication Synthesis	5	
12	11/6, 11/8	High-Level Synthesis I	6	HW #3
13	11/13, 11/15	High-Level Synthesis II	6	
14	11/20, ~~11/22~~	Verification	7	
15	11/27, 11/29	Final Exam Review		
16	TBD	**Final Exam**		