ECE 587 – Hardware/Software Co-Design
Fall 2009

Instructor: Professor Jia Wang
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Prerequisite: Fundamentals of logic design and computer architecture. Microprocessor, microcontroller and ASIC design. Familiarity with VHDL or Verilog hardware description languages.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Thur. 6:25PM – 9:05PM
Class Location: Life Sciences 121
Class Home Page: `http://blackboard.iit.edu/`

Office Hrs: Fri. 10:00 AM – 12:00 Noon, SH 317; or by appointment

Required Textbook:

- "Specification and Design of Embedded Systems"
  Daniel D. Gajski, Frank Vahid, Sanjiv Narayan, Jie Gong, Prentice Hall, 1994.
  ISBN-13: 978-0131507319. ISBN-10: 0131507311.
- Plus additional notes

Course Objective: To give students a clear understanding of the modern methodology for the hardware/software co-design of embedded systems.

Topics Covered: General design methodology; functional specification and verification; hardware/software partitioning; design quality analysis; system synthesis and optimization

Grading: Homeworks: 10% / Project(s): 20% / Midterm Exam: 30% / Final Exam: 40% / Class Participation: 5% (Extra). A: $\geq$ 90% / B: $\geq$ 80% / C: $\geq$ 60%.

Teaching Assistants: Joshua Weber, `jweber8@iit.edu`, Tue. 2:00 PM – 4:00 PM, SH 302

Homework and Project Policy: Late homeworks and project reports will not be accepted. Discussions on homeworks/projects is encouraged, but copying will call for disciplinary action.

Final Exam Policy: Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

No.	Date	Topic	Chapters	HW & Project
1	8/27	Introduction	1	
2	9/3	Models and Architectures	2	
3	9/10	Specification Languages	3, 4	HW #1
4	9/17	Translation to VHDL	5	
5	9/24	Transaction Level Modeling	Notes	PRJ #1
6	10/1	System Partitioning I	6, Notes	
7	10/8	System Partitioning II	6, Notes	HW #2
8	10/15	**Midterm Exam**		
9	10/22	Design Quality Estimation I	7, Notes	PRJ #2
10	10/29	Design Quality Estimation II	7, Notes	HW #3
11	11/5	Specification Refinement I	8	
12	11/12	Specification Refinement II	8	HW #4
13	11/19	Multiprocessor System-on-Chip	Notes	
14	11/26	**Thanksgiving Holiday**		
15	12/3	System-Design Methodology	9	
16	TBD	**Final Exam**		