ECE 586 – Fault Detection in Digital Circuits
Lecture 21 Design for Testability III

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This lecture: 9.8 – 9.10
Next lecture: 10.1 – 10.5
Board-Level and System-Level DFT Approaches

Boundary-Scan Standards
System-Level Busses

Figure 9.34  System-level test using system bus

(Abramovici et al., 1990)
System-Level Scan Paths

(Abramovici et al., 1990)
Multiple Test Session

Together mode: Need $100 \times 12 = 1200$ cycles.

Separate mode: need $100 \times 8 + 20 \times 8 = 960$ cycles.

Overlapped mode: need $20 \times 12 + 80 \times 8 = 880$ cycles.

Figure 9.36  Testing using multiple test sessions

(Abramovici et al., 1990)
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In essence, registers/DFFs can be moved (retimed) together to simplify the scan design via I-Path.
Different partial scan designs may have different costs since the registers may have different widths.
Outline

Board-Level and System-Level DFT Approaches

Boundary-Scan Standards
Chip Architecture for IEEE 1149.1

(Fig. 9.45, Abramovici et al., 1990)
Test Bus Explained

- A processor specialized for testing.
- TCK: Test Clock.
- Datapath
  - TDI: Test Data Input.
  - TDO: Test Data Output.
- Controller: TAP
  - TMS: Test Mode Selector. Input to the TAP FSM.
Test Bus Explained

- A processor specialized for testing.
- **TCK**: Test Clock.
  - **Datapath**
    - **TDI**: Test Data Input.
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Board Configuration

(Fig. 9.47, Abramovici et al., 1990)
System Configurations

Figure 9.51  (a) Ring configuration (b) Star configuration

(Abramovici et al., 1990)
Normal mode: Mode_Control=0, send IN to OUT

Scan mode: ShiftDR=1, send SIN to SOUT

Capture mode: ShiftDR=0, save IN to QA

Update mode: Mode_Control=1, send QA to OUT
Boundary-Scan Cell Design

(Fig. 9.46(b), Abramovici et al., 1990)

- Normal mode: $\text{Mode\_Control}=0$, send $IN$ to $OUT$
- Scan mode: $\text{ShiftDR}=1$, send $SIN$ to $SOUT$
- Capture mode: $\text{ShiftDR}=0$, save $IN$ to $Q_A$
- Update mode: $\text{Mode\_Control}=1$, send $Q_A$ to $OUT$
Boundary-Scan Cell Design

▶ Normal mode: Mode_Control=0, send IN to OUT
▶ Scan mode: ShiftDR=1, send SIN to SOUT
▶ Capture mode: ShiftDR=0, save IN to QA
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(Fig. 9.46(b), Abramovici et al., 1990)
Boundary-Scan Cell Design

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- **Normal mode:** Mode_Control = 0, send IN to OUT
- **Scan mode:** ShiftDR = 1, send SIN to SOUT
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External Test Mode

▶ Test interconnects and logic external to chips.

(Fig. 9.48, Abramovici et al., 1990)
Sample Test Mode

Sample I/O data during normal system operation.

(Fig. 9.49, Abramovici et al., 1990)
Test internal application logic.

(Fig. 9.50, Abramovici et al., 1990)
The challenge of board-level and system-level DFT approaches is to enable testing of the individual components and the whole system without reconfiguration of the interconnects.

Boundary-scan standards define the ways to access chips for testing (controllability and observability) in a programmable manner.