ECE 586 – Fault Detection in Digital Circuits
Fall 2013

Instructor: Professor Jia Wang
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Prerequisite:
ECE 446 Design and analysis of combinational and synchronous sequential logics.

Though not required, you are recommended to take ECE 449 before taking this course.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Tue./Thur. 5:00 PM – 6:15 PM
Class Location: Stuart Building 107
Class Home Page: `http://www.ece.iit.edu/~jwang/ece586-2013f/`

Office Hrs: TBD

Required Textbook: "Digital Systems Testing and Testable Designs"
M. Abramovici, M. A. Breuer, A. D. Friedman, IEEE Press, 1990.
ISBN: 0-7803-1062-4 (eBook available from `http://library.iit.edu/`)

Recommended Textbook: "VLSI Test Principles and Architectures: Design for Testability"
L.-T. Wang, C.-W. Wu, X. Wen, Elsevier Inc., 2006. ISBN: 978-0-12-370597-6

Course Objective: To give students a clear understanding of digital design testing and testability, and to promote independent problem solving via algorithmic techniques.

Topics Covered: circuit and logic models; logic and fault simulations; automatic test pattern generation; design for testability; test compression; built-in self-test.

Grading: Homeworks: 30% / Literature Survey: 30% / Final Exam: 40% / Bonus Project: 40% (Extra). A: $\geq$ 90% / B: $\geq$ 75% / C: $\geq$ 60%.

Teaching Assistants: TBD

Homework and Project Policy: Late homeworks and projects will not be graded. Deadlines will NOT be extended, except for extraordinary reasons. Homeworks will be graded based on general approach and completion, and solutions will be released shortly after due date. Discussions on homeworks/projects are encouraged, but copying will call for disciplinary action.

Exam Policy: Close book, close note, cheat sheet allowed. Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

No.	Date	Topic	Chapters	HW & Project Out
1	8/20, 8/22	Introduction	1	
2	8/27, 8/29	Functional Models	2	
3	9/3, 9/5	Structural Models	2	HW #1
4	9/10, 9/12	Logic Simulation I	3	
5	9/17, 9/19	Logic Simulation II	3	HW #2
6	9/24, 9/26	Fault Modeling	4	
7	10/1, 10/3	Fault Simulation I	5	Bonus Project
8	10/8, 10/10	Fault Simulation II	5	HW #3
9	10/15, 10/17	Testing for SSF I	6	
10	10/22, 10/24	Testing for SSF II	6	HW #4
11	10/29, 10/31	Design for Testability	9	
12	11/5, 11/7	Compression Techniques	10	HW #5
13	11/12, 11/14	Built-In Self-test	11	
14	11/19, 11/21	Functional Testing	8	
15	11/26, ~~11/28~~	Final Exam Review		
16	12/3 (Tue.)	**Final Exam 5:00 PM – 7:00 PM**		