

ECE 585 – Advanced Computer Architecture Spring 2009

Instructor: Professor Jia Wang

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Prerequisite: Combinational and sequential circuit design. Computer programming. Experience with Verilog/VHDL and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or disabilities@iit.edu.

Class Time: Tue. 6:25PM – 9:05PM

Class Location: Engineering 1, Room 104

Class Home Page: <http://blackboard.iit.edu/>

Office Hrs: Tue. 2:00 PM – 4:00 PM, SH 317 (tentative) or by appointment

Required Textbook:

QA4 “Computer Architecture: A Quantitative Approach” (4th ed.)

John L. Hennessy and David A. Patterson, Morgan Kaufmann, 2007.

ISBN-13: 978-0123704900. ISBN-10: 0123704901.

HSI3 “Computer Organization and Design: The Hardware/Software Interface” (3rd ed.)

David A. Patterson and John L. Hennessy, Morgan Kaufmann, 2007.

ISBN-13: 978-0123706065. ISBN-10: 0123706068.

Notes Additional notes.

Course Objective: To give students a clear understanding of the modern computer architecture and the trend in computer architecture research. Students will learn the design and analysis of complex and high performance (multi)processors and supporting subsystems from the quantitative aspect.

Topics Covered: Instruction set design; pipelining; instruction-level parallelism; memory hierarchy design; disk storage; networking; process scheduling; thread-level parallelism; cache coherence; transactional memory.

Grading: Homeworks 10% / Final Exam: 40%/ Projects: 50% / Class Participation (Extra 5%)

Teaching Assistants: Joshua Weber jweber8@iit.edu

Homework and Project Policy: Late homeworks and project reports will not be accepted. Discussions on homeworks/projects is encouraged, but copying will call for disciplinary action.

Final Exam Policy: Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

No.	Date	Topic	Chapters	HW & Project
1	1/21	MIPS and Its Basic Implementation	HSI3: 2, 5.1–5.4 HSI4: 2, 4.1–4.4	
			QA3: 2 QA4: B.1–B.9	
2	1/27	Pipelining and Hazards	HSI3: 6.1–6.6, 6.8 HSI4: 4.5–4.9	HW #1
			QA3: A.1–A.6 QA4: A.1–A.6	
3	2/3	Introduction to ILP	QA3: 3.1, 4.1 QA4: 2.1–2.2	
4	2/10	Branch Prediction	QA3: 3.4, 4.2 QA4: 2.3	
5	2/17	Dynamic Scheduling	QA3: A.8, 3.2–3.3 QA4: A.7, 2.4–2.5	HW #2
6	2/24	Hardware-Based Speculation	QA3: 3.7 QA4: 2.6	PRJ #1 Due
7	3/3	ILP Overview and Implementation	QA3: 3.5–3.6, 4.3 QA4: 2.7–2.10	
			Notes	
8	3/10	Memory Hierarchy I	HSI3: 7.1–7.5 HSI4: 5.1–5.5	
			QA3: 5.2–5.7, 5.10–5.11 QA4: C.1–C.5	
9	3/17	Spring Break		
10	3/24	Memory Hierarchy II	QA3: 5.1, 5.4–5.9, 5.12 QA4: 5.1–5.6	HW #3
11	3/31	Storage System	HSI3: 8.1–8.2, 8.4–8.7 HSI4: 6.1–6.9	PRJ #2 Due
			QA3: 7.1–7.10 QA4: 6.1–6.6	
12	4/7	Networking	HSI3: 8.3 HSI4: 6.11	HW #4
			QA3: 8 QA4: E	
13	4/14	Process Scheduling	Notes	
14	4/21	Multiprocessor and Cache Coherence	QA3: 6.1–6.6 QA4: 4.1–4.4	HW #5
15	4/28	Memory Consistency	QA3: 6.7–6.8, 6.10 QA4: 4.5–4.7	
16	5/5	Transactional Memory	Notes	PRJ #3 Due
17	TBD	Final Exam		
QA3: “Computer Architecture: A Quantitative Approach”, 3rd ed.				
QA4: “Computer Architecture: A Quantitative Approach”, 4th ed.				
HSI3: “Computer Organization and Design: The Hardware/Software Interface”, 3rd ed.				
HSI4: “Computer Organization and Design: The Hardware/Software Interface”, 4th ed.				