ECE 429 – Introduction to VLSI Design
Spring 2017

Instructor: Professor Jia Wang
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Prerequisite: ECE 218 and ECE 311
Familiarity with circuits, logic and digital system design.
Experience with CAD tools and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Tue./Thur.: 3:15 PM – 4:30 PM
Class Location: Wishnick Hall 113
Class Home Page: `http://www.ece.iit.edu/~jwang/ece429-2017s/`

Office Hrs: TBD

Required Textbook: "CMOS VLSI DESIGN: A Circuits and Systems Perspective" 4th ed.
Neil H.E. Weste and David Harris, Addison-Wesley. ISBN: 0321547748

Course Objective: To give students a clear understanding of the fundamental concepts of modern CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems from register-transfer level to circuit level.

Topics Covered: MOS transistors, MOS layout and fabrication, CMOS gate design, wire engineering, timing and power analysis, combinational and sequential circuit design, data-path and control unit design, memory design, ASIC design flow.

Grading: Homeworks 10% / Midterm Exam: 15% / Final Exam: 35% / Labs and Projects: 40% / Class Participation 5% (Extra). A: $\geq 90\%$ / B: $\geq 80\%$ / C: $\geq 60\%$ / D (undergraduate only): $\geq 55\%$.

Teaching Assistants: TBD

Homework and Lab/Project Report Policy: Late homeworks and reports will not be graded. Deadlines will NOT be extended, except for extraordinary reasons. Homeworks will be graded based on general approach and completion, and solutions will be released shortly after due date. Discussions are encouraged, but copying will call for disciplinary action.

Exam Policy: Close book, close note, cheat sheet allowed. Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

No.	Date	Topic	Chapters	HW	Lab & Project
1	1/10, 1/12	Introduction	1		No Lab
2	1/17, 1/19	MOS Transistor Theory	1,2	#1	Lab 1: Lab Setup
3	1/24, 1/26	Static CMOS Design and Layout	3		Lab 2: Inverter Schematic
4	1/31, 2/2	Timing I	4	#2	Lab 3: Inverter Layout
5	2/7, 2/9	Timing II, Power	4,5		Lab 4: Gate Delay and Power
6	2/14, 2/16	Interconnect	6	#3	Lab 5: Hierarchical Design and Formal Verification
7	2/21, 2/23	Combinational Circuit Design	9		Lab 6: Carry-Ripple Addition I
8	2/28, 3/2	Midterm Review, Verilog	A		Lab 7: Carry-Ripple Addition II
9	3/7	**Midterm Exam**			Lab 8: Carry-Ripple Addition III
	3/9	ASIC Design Flow	14		
10	~~3/14~~, ~~3/16~~	**Spring Break**			
11	3/21, 3/23	Sequential Circuit Design I, Final Project Introduction	10,1	#4	Lab 9: ASIC Design Flow
12	3/28, 3/30	Sequential Circuit Design II	10		Final Project I
13	4/4, 4/6	Adder Design	11	#5	Final Project II
14	4/11, 4/13	Memory Design	12		Final Project II
15	4/18, 4/20	Robustness, Final Review	7,13		Final Project II
16	4/25, 4/27	**Final Project Demonstration**			
17	5/1–5/5	**Final Exam**			

Course Objectives (ABET)
After completing this course, the student should be able to do the following:

1. Design VLSI circuits from register-transfer level to layouts.
2. Discuss the basic attributes of VLSI systems, their impact upon society, and the tradeoffs between design metrics, especially speed, power, and cost.
3. Design experiments to measure design metrics and explain the differences between theoretical models and experiments.
4. Identify the basic parts of VLSI design flows. Compare/contrast both custom and standard-cell based design methodologies.
5. Explain and analyze dynamic techniques such as charge sharing and current leakage and how it impacts specific circuits from a dynamic circuits perspective.
6. Complete an engineering design incorporating engineering standards and realistic constraints.
7. Prepare an informative and organized design project report with solid supporting data and deliver an oral presentation.