ECE 429 – Introduction to VLSI Design
Spring 2016

Instructor: Professor Jia Wang
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Prerequisite: ECE 218 and ECE 311
Familiarity with circuits, logic and digital system design.
Experience with CAD tools and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to
receive accommodations, students must obtain a letter of accommodation from the Center for Disability
Resources and make an appointment to speak with me as soon as possible. The Center for Disability
Resources is located in the Life Sciences Building, room 218, 312-567-5744 or disabilities@iit.edu.

Class Time: Mon./Wed.: 10:00 AM – 11:15 AM
Class Location: Wishnick Hall 115
Class Home Page: http://www.ece.iit.edu/~jwang/ece429-2016s/

Office Hrs: TBD

Neil H.E. Weste and David Harris, Addison-Wesley. ISBN: 0321547748

Course Objective: To give students a clear understanding of the fundamental concepts of modern
CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems
from register-transfer level to circuit level.

Topics Covered: MOS transistors, MOS layout and fabrication, CMOS gate design, wire engineering,
timing and power analysis, combinational and sequential circuit design, data-path and control unit
design, memory design, ASIC design flow.

Grading: Homeworks 10% / Midterm Exam: 20% / Final Exam: 30% / Labs and Projects: 40% /
Class Participation 5% (Extra). A: ≥ 90% / B: ≥ 80% / C: ≥ 60% / D (undergraduate only): ≥ 55%.

Teaching Assistants: TBD

Homework and Lab/Project Report Policy: Late homeworks and reports will not be graded.
Deadlines will NOT be extended, except for extraordinary reasons. Homeworks will be graded based
on general approach and completion, and solutions will be released shortly after due date. Discussions
are encouraged, but copying will call for disciplinary action.

Exam Policy: Close book, close note, cheat sheet allowed. Makeup exams will NOT be given, except
for extraordinary reasons.
Lecture Schedule (tentative):

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<th>Topic</th>
<th>Chapters</th>
<th>HW</th>
<th>Lab &amp; Project</th>
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<td>No Lab</td>
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<td>2</td>
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<td>Power</td>
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<td>Lab 4: Gate Delay and Power</td>
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<td>Interconnect</td>
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<td>2/22, 2/24</td>
<td>Verilog, Midterm Review</td>
<td>A</td>
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<td>2/29, 3/2</td>
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<td>Lab 7: Carry-Ripple Addition II</td>
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Midterm Exam

| 9   | 3/7, 3/9     | Combinational Circuit Design II, ASIC Design Flow | 9, 14 |     | Lab 8: Carry-Ripple Addition III |
| 10  | 3/14, 3/16   | Spring Break                          |        |     |                          |
| 12  | 3/28, 3/30   | Sequential Circuit Design II          | 10      |     | Final Project I           |
| 13  | 4/4, 4/6     | Adder Design                          | 11      | #5  | Final Project II          |
| 14  | 4/11, 4/13   | Memory Design                         | 12      |     | Final Project II          |
| 15  | 4/18, 4/20   | Testing and Verification              | 15      |     | Final Project II          |
| 16  | 4/25, 4/27   | Final Review, Robustness              | 7, 13   |     | Final Project Demonstration |
| 17  | 5/2–5/7      |                                       |         |     | Final Exam                |

Course Objectives (ABET)

After completing this course, the student should be able to do the following:

1. Design VLSI circuits from register-transfer level to layouts.
2. Discuss the basic attributes of VLSI systems, their impact upon society, and the tradeoffs between design metrics, especially speed, power, and cost.
3. Design experiments to measure design metrics and explain the differences between theoretical models and experiments.
4. Identify the basic parts of VLSI design flows. Compare/contrast both custom and standard-cell based design methodologies.
5. Explain and analyze dynamic techniques such as charge sharing and current leakage and how it impacts specific circuits from a dynamic circuits perspective.
6. Complete an engineering design incorporating engineering standards and realistic constraints.
7. Prepare an informative and organized design project report with solid supporting data and deliver an oral presentation.