ECE 429 – Introduction to VLSI Design
Fall 2011

Instructor: Professor Jia Wang
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Prerequisite: ECE 218 and ECE 311
Familiarity with circuits, logic and digital system design.
Experience with CAD tools and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Thur.: 6:25 PM – 9:05 PM
Class Location: Perlstein Hall – Room 131
Class Home Page: `http://blackboard.iit.edu/`

Office Hrs: TBD

Required Textbook: "CMOS VLSI DESIGN: A Circuits and Systems Perspective" 4th ed.
Neil H.E. Weste and David Harris, Addison-Wesley. ISBN: 0321547748

Course Objective: To give students a clear understanding of the fundamental concepts of modern CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems from circuit level to system level.

Topics Covered: MOS transistors, MOS layout and fabrication, CMOS gate design, wire engineering, timing and power analysis, combinational and sequential circuit design, data-path and control unit design, memory design, ASIC design flow.

Grading: Homeworks 10% / Midterm Exam: 20% / Final Exam: 30% / Labs and Project: 40% / Class Participation 5% (Extra). A: $\geq 90\%$ / B: $\geq 75\%$ / C: $\geq 60\%$ / D (undergraduate only): $\geq 55\%$.

Teaching Assistants: TBD

Homework and Project Policy: Late homeworks and lab/project reports will not be graded. Discussions on homeworks/labs/projects are encouraged, but copying will call for disciplinary action.

Final Exam Policy: Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

Date	Topic	Chapters	HW	Lab & Project
8/25	Introduction, CMOS Inverter	1, 2	#1	Lab 1: Lab Setup
9/1	Static CMOS Design, CMOS Fabrication	3, 1		Lab 2: Inverter Schematic
9/8	Gate Delay	4	#2	Lab 3: Inverter Layout
9/15	Power	5		Lab 4: Gate Delay and Power
9/22	Interconnect	6	#3	Lab 5: Hierarchical Design and Formal Verification
9/29	Combinational Circuit Design	9		Lab 6: Carry-Ripple Addition I
10/6	Verilog, Midterm Review	A		Lab 7: Carry-Ripple Addition II
10/13	**Midterm Exam**			
10/20	Sequential Circuit Design I, ASIC Design Flow	10, 14	#4	Lab 8: Carry-Ripple Addition III
10/27	Sequential Circuit Design II, Final Project Introduction	10, 1		Lab 9: ASIC Design Flow
11/3	Adder	11	#5	Final Project I
11/10	Memory	12		Final Project II
11/17	Testing and Verification	15		Final Project II
11/24	**Thanksgiving**			
12/1	Robustness, Final Review	7, 13		Final project demonstration
12/5–12/9	**Final Exam**			