Instructor: Professor Jia Wang  
Office: 317 Siegel Hall  
Phone: 312-567-3696  
E-Mail: jwang@ece.iit.edu (Please start your email subject line with [ECE429].)

Prerequisite: ECE 218 and ECE 311  
Familiarity with circuits, logic and digital system design.  
Experience with CAD tools and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or disabilities@iit.edu.

Class Time: Thur.: 6:25 PM – 9:05 PM  
Class Location: Perlstein Hall – Room 131  
Class Home Page: http://blackboard.iit.edu/

Office Hrs: TBD

Neil H.E. Weste and David Harris, Addison-Wesley. ISBN: 0321547748

Course Objective: To give students a clear understanding of the fundamental concepts of modern CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems from circuit level to system level.

Topics Covered: MOS transistors, MOS layout and fabrication, CMOS gate design, wire engineering, timing and power analysis, combinational and sequential circuit design, data-path and control unit design, memory design, ASIC design flow.

Grading: Homeworks 10% / Midterm Exam: 20% / Final Exam: 30% / Labs and Project: 40% / Class Participation 5% (Extra). A: ≥ 90% / B: ≥ 75% / C: ≥ 60% / D (undergraduate only): ≥ 55%.

Teaching Assistants: TBD

Homework and Project Policy: Late homeworks and lab/project reports will not be graded. Discussions on homeworks/labs/projects are encouraged, but copying will call for disciplinary action.

Final Exam Policy: Makeup exams will NOT be given, except for extraordinary reasons.
### Lecture Schedule (tentative):

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