# ECE 429 – Introduction to VLSI Design
# Spring 2010

**Instructor:** Professor Jia Wang
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**Prerequisite:** ECE 218 and ECE 311
Familiarity with circuits, logic and digital system design.
Experience with CAD tools and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

**Class Time:** Tues. and Thur.: 3:15 PM – 4:30 PM
**Class Location:** Perlstein Hall – Room 131
**Class Home Page:** `http://blackboard.iit.edu/`

**Office Hrs:** TBD

**Required Textbook:** "CMOS VLSI DESIGN: A Circuits and Systems Perspective" (3rd ed.)
Neil H.E. Weste, and David Harris, Addison-Wesley, 2005. ISBN: 0321149017
*Warning: As some international editions are different from the original book on technical contents and homework questions, please make sure your purchase matches the original one.*

**Course Objective:** To give students a clear understanding of the fundamental concepts of modern CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems from system level to circuit level.

**Topics Covered:** MOS transistors, static and dynamic behavior, stick diagrams, MOS circuit fabrication, design rules, resistance and capacitance extraction, scaling, logical effort, combinational and sequential design, data-path and control unit design, clocking schemes, memory design. CAD synthesis techniques, floorplanning and layout.

**Grading:** Homeworks 10% / Midterm Exam: 20% / Final Exam: 30% / Labs and Project: 40% / Class Participation 5% (Extra). A: $\geq$ 90% / B: $\geq$ 80% / C: $\geq$ 60%.

**Teaching Assistants:** TBD

**Homework and Project Policy:** Late homeworks and project reports will not be accepted. Discussions on homeworks/projects are encouraged, but copying will call for disciplinary action.

**Final Exam Policy:** Makeup exams will NOT be given, except for extraordinary reasons.

**Lecture Schedule (tentative):**

| Date | Topic | Chapters | HW | Lab & Project |
|---|---|---|---|---|
| 1/12, 1/14 | Introduction, Device Physics | 1, 2 | | |
| 1/19, 1/21 | CMOS Inverter and Fabrication | 2, 3 | #1 | Lab 1: basic unix |
| 1/26, 1/28 | CMOS Logic and Layout, Delay | 3, 4 | | Lab 2: inverter schemetic |
| 2/2, 2/4 | Sizing and Logical Effort | 4 | #2 | Lab 3: HSPICE |
| 2/9, 2/11 | Interconnect and Wire Engineering | 4 | | Lab 4: layout editor |
| 2/16, 2/18 | Power, Midterm Review | 4 | #3 | Lab 5: CMOS design flow |
| 2/23 | Static CMOS and Pass-Transistor Circuits | 6 | | Lab 6: CMOS logic gate design |
| 2/25 | **Midterm Exam** | | | |
| 3/2, 3/4 | Dynamic Circuits, Verilog HDL | 6, A | | Lab 7: bit-slice addition and subtraction |
| 3/9, 3/11 | **Spring Break** | | | |
| 3/16, 3/18 | Sequential Circuit Design, ASIC Design Flow | 7, 8 | #4 | Lab 8: Verilog HDL |
| 3/23, 3/25 | Clock Scheduling, Final Project | 7, 1 | | Lab 9: synthesis flow for D-register |
| 3/30, 4/1 | Adder Design | 10 | #5 | Final project part I |
| 4/6, 4/8 | Datapath, Memory | 10, 11 | | Final project part II |
| 4/13, 4/15 | Programmable Arrays, Testing | 11, 8, 9 | | Final project part II |
| 4/20, 4/22 | Scaling and Reliability | 4, 12 | | Final project part II |
| 4/27, 4/29 | Final Review, Introduction to VLSI CAD | 5 | | Final project demonstration |
| 5/3–5/8 | **Final Exam** | | | |