ECE 429 – Introduction to VLSI Design
Fall 2010

Instructor: Professor Jia Wang
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Prerequisite: ECE 218 and ECE 311
Familiarity with circuits, logic and digital system design.
Experience with CAD tools and UNIX is a plus.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time: Thur.: 6:25 PM – 9:05 PM
Class Location: Life Sciences – Room 111
Class Home Page: `http://blackboard.iit.edu/`

Office Hrs: TBD

Required Textbook: "CMOS VLSI DESIGN: A Circuits and Systems Perspective" (3rd ed.)
Neil H.E. Weste, and David Harris, Addison-Wesley, 2005. ISBN: 0321149017
Warning: As some international editions are different from the original book on technical contents and homework questions, please make sure your purchase matches the original one.
Note: 4th ed. of the above book (ISBN:0321547748) is acceptable.

Course Objective: To give students a clear understanding of the fundamental concepts of modern CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems from system level to circuit level.

Topics Covered: MOS transistors, static and dynamic behavior, stick diagrams, MOS circuit fabrication, design rules, resistance and capacitance extraction, scaling, logical effort, combinational and sequential design, data-path and control unit design, clocking schemes, memory design. CAD synthesis techniques, floorplanning and layout.

Grading: Homeworks 10% / Midterm Exam: 20% / Final Exam: 30% / Labs and Project: 40% / Class Participation 5% (Extra). A: $\geq 90\%$ / B: $\geq 75\%$ / C: $\geq 60\%$ / D (undergraduate only): $\geq 55\%$.

Teaching Assistants: TBD

Homework and Project Policy: Late homeworks and lab/project reports will not be graded. Discussions on homeworks/labs/projects are encouraged, but copying will call for disciplinary action.

Final Exam Policy: Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

Date	Topic	Chapters	HW	Lab & Project
8/26	Introduction, CMOS Inverter	1, 2	#1	Lab 1: Basic Unix
9/2	CMOS Fabrication, Static CMOS Design	3, 1		Lab 2: Inverter Schematic
9/9	Gate Delay and Logical Effort	4	#2	Lab 3: HSPICE Simulation
9/16	Interconnect	4		Lab 4: Inverter Layout
9/23	Power Dissipation, Reliability	4	#3	Lab 5: CMOS Gate Design I
9/30	Combinational Circuit Design	6		Lab 6: CMOS Gate Design II
10/7	Verilog HDL, Midterm Review	A		Lab 7: CMOS Circuit Design
10/14	**Midterm Exam**			
10/21	Sequential Circuit Design I, ASIC Design Flow	7, 8	#4	Lab 8: Verilog HDL
10/28	Sequential Circuit Design II, Final Project	7, 1		Lab 9: ASIC Design Flow
11/4	Adder Design	10	#5	Final Project I
11/11	Datapath, Memory	10, 11		Final Project II
11/18	Programmable Arrays, Testing	11, 8, 9		Final Project II
11/25	**Thanksgiving**			
12/2	Power and Clock Distribution, Final Review	12		Final project demonstration
12/6–12/10	**Final Exam**			