ECE 429 – Introduction to VLSI Design
Fall 2008

Instructor: Professor Jia Wang
Office: 133 Siegel Hall (temporary)
Phone: 312 567-3907 (temporary)
E-Mail: jwang@ece.iit.edu (Please start your email subject line with [ECE429].)

Prerequisite: ECE 218 and ECE 311
Familiarity with circuits, logic and digital system design.
Experience with CAD tools and UNIX is a plus.

Class Time: Tues. and Thur.: 10:00 AM – 11:15 AM
Class Location: Perlstein Hall – Room 131

Office Hrs: Tues. and Thur.: 2:00 PM – 3:00 PM, SH 133 (tentative) or by appointment

Class Home Page: `http://blackboard.iit.edu/` → log in → choose "INTRO TO VLSI DESIGN"

Required Textbook: "CMOS VLSI DESIGN: A Circuits and Systems Perspective" (3rd ed.)
Neil H.E. Weste, and David Harris, Addison-Wesley, 2005. ISBN: 0321149017

Course Objective: To give students a clear understanding of the fundamental concepts of modern CMOS VLSI design. Students will learn the design of complex and high performance CMOS systems from system level to circuit level.

Topics Covered: MOS transistors, static and dynamic behavior, stick diagrams, MOS circuit fabrication, design rules, resistance and capacitance extraction, scaling, logical effort, combinational and sequential design, data-path and control unit design, clocking schemes, memory design. CAD synthesis techniques, floorplanning and layout.

Grading: Homeworks 10% / Midterm Exam: 20% / Final Exam: 30% / LABs and Project: 40% / Class Participation (Extra 5%)

Teaching Assistants: TBD

Homework Policy: Homework is due at the start of class. Late homework will not be accepted. Working together on homework is encouraged, but copying assignments will call for disciplinary action. For the project, you may be asked to work in groups.

Exam Policy: Makeup exams will not be given, except for extraordinary reasons. The final is comprehensive.

Recommended books: Not required, hand-out will be given in the class.

Lecture Schedule (tentative):

Date	Topic	Related Chapters	HW	Lab & Project
8/21	Overview and VLSI Design Flow	1.1–1.3, 8.1–8.4		
8/26, 8/28	MOS Transistor Theory	2.1–2.6		
9/2, 9/4	CMOS Fabrication, Layout, Processing Technology	1.5, 3.1–3.6	#1	Lab 1: basic unix
9/9, 9/11	Delay Estimation	4.2		Lab 2: inverter schemetic
9/16, 9/18	Logical Effort	4.3	#2	Lab 3: HSPICE
9/23, 9/25	Power Estimation	4.4		Lab 4: layout editor
9/30, 10/2	Interconnect	4.5	#3	Lab 5: CMOS design flow
10/7, 10/9	Circuit Simulation and Review for Midterm	5.1–5.5		Lab 6: CMOS logic gate design
10/14	**Midterm Exam**			
10/16	**Fall Break**			
10/21, 10/23	Combinational Circuit Design	6.2	#4	Lab 7: bit-slice addition and subtraction
10/28, 10/30	Sequential Circuit Design	7.2, 7.3		Lab 8: Verilog HDL
11/4, 11/6	Adders and Final Project	10.1, 10.2	#5	Lab 9: synthesis flow for D-register
11/11, 11/13	Datapath Functional Units	10.3–10.9		Final project part I
11/18, 11/20	Memories I	11.1, 11.2		Final project part II
11/25	Memories II	11.3–11.5		Final project part II
11/27	**Thanksgiving**			
12/2, 12/4	Design for Testability and Review for Final Exam	9.6		Final project demonstration
12/8–12/13	**Final Exam**			