ECE 218 – Digital Systems
Spring 2013

Instructor: Professor Jia Wang
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Prerequisites: None.
Concurrent registration in ECE 211 and ECE 212 is strongly encouraged.

Reasonable accommodations will be made for students with documented disabilities. In order to receive accommodations, students must obtain a letter of accommodation from the Center for Disability Resources and make an appointment to speak with me as soon as possible. The Center for Disability Resources is located in the Life Sciences Building, room 218, 312-567-5744 or `disabilities@iit.edu`.

Class Time and Location: Tue. and Thurs.: 11:25 AM – 12:40 PM Perlstein Hall 108
Class Home Page: `http://blackboard.iit.edu/`

Required Textbook:
"Digital Design", 4th ed, M. Morris Mano and M.D. Ciletti,
Pearson Prentice Hall, 2006. ISBN: 978-0131989245

Course Objective: To give students a clear understanding of the digital design techniques, with emphasis on combinational logic designs and synchronous sequential logic designs.

Topics Covered: Number systems and conversions, binary codes, and Boolean algebra. Switching devices, discrete and integrated digital circuits, analysis and design of combinational logic circuits. Karnaugh maps and minimization techniques. Counters and registers. Analysis and design of synchronous sequential circuits.

Grading: Homeworks 15% / Midterm 30% / Final Exam 45% / Class Participation 10%. A: $\geq$ 90% / B: $\geq$ 80% / C: $\geq$ 70% / D: $\geq$ 60%.

Homework Policy: Late homeworks will not be graded. Deadlines will NOT be extended, except for extraordinary reasons. Homeworks will be graded based on general approach and completion, and solutions will be released shortly after due date. Discussions on homeworks are encouraged, but copying will call for disciplinary action.

Exam Policy: Close book, close note, cheat sheet allowed. Makeup exams will NOT be given, except for extraordinary reasons.

Lecture Schedule (tentative):

Date	Topic	Chapters	HW Out
1/15, 1/17	Digital Systems	1.1–1.4, 1.7, 2.9	
1/22, 1/24	Boolean Algebra I: Basic Operations	2.1–2.4	HW#1
1/29, 1/31	Boolean Algebra II: Boolean Functions	2.5–2.6	
2/5, 2/7	Combinational Logic I: Two-Level Logic	2.7, 2.8, 3.1–3.3	HW#2
2/12, 2/14	Combinational Logic II: beyond Sum-of-Products	3.5–3.7, 3.9	
2/19, 2/21	Combinational Logic III: Multi-Level Logic	4.1–4.4, 4.9, 4.10	HW#3
2/26, 2/28	Combinational Logic IV: Multiplexer	4.11	
3/5, 3/7	**Review/Midterm Exam**		
3/12, 3/14	Combinational Logic V: Addition and Subtraction	1.5, 1.6, 4.5, 4.8	HW#4
~~3/19~~, ~~3/21~~	**Spring Break**		
3/26, 3/28	Synchronous Sequential Logic I: Finite State Machine	5.1, 5.2, 5.4, 5.5	
4/2, 4/4	Synchronous Sequential Logic II: Registers and Counters	6.1–6.5	HW#5
4/9, 4/11	Synchronous Sequential Logic III: Program to RTL	8.1, 8.2, 8.4, 8.5, 8.7, 8.8	
4/16, 4/18	Memory Array	7.1–7.3, 7.5	HW#6
4/23, 4/25	Programmable Logic	7.6–7.8	
4/30, 5/2	Discussions and Review		
5/6 – 5/10	**Final Exam**		