Vectorless Verification of RLC Power Grids with Transient Current Constraints

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***Abstract*—Vectorless power grid verification is a powerful method that evaluates worst-case voltage noises without detailed current waveforms using optimization techniques. It is extremely challenging when considering RLC power grids since inductors are difficult to tackle and multiple time steps should be evaluated after the discretization of the system equation. In this paper, we study integrated RLC power grids with both VDD and GND networks and rigorously prove that their vectorless verification can be decomposed into two sub-problems – the well-studied transient power grid analysis problem and an optimization problem that maximizes an affine function of currents under current constraints. We further introduce transient constraints to restrict the waveform of each current source for realistic scenarios and design the RLCVN algorithm to solve the vectorless verification problem of RLC power grids. Results confirm that our algorithm is an effective approach for practical RLC power grid verification, and the proposed transient constraints make the noise estimations more realistic.**

I. Introduction

As the development of deep sub-micron technologies, the decreasing circuit supply voltage and the transistor threshold voltage make modern chips increasingly vulnerable to power supply noises, i.e. IR drops and Ldi/dt noises on power girds. Such voltage noises are critical in modern chip designs, because they may lead to insufficient supply voltage at gates or cells, resulting in logic errors or longer delays. Hence, power grid verification is indispensable in modern design flow to ensure a reliable high-speed chip design.

Most available power grid verification algorithms are based on simulation. Typically, the power gird is modeled as an RC/RLC circuit with current sources, which represent the current drawn by the underlying circuitry. Using waveforms of current sources, one can simulate the power grid to evaluate nodal voltages. Lots of algorithms have been proposed for fast simulation of power grids [1], [2], [3], [4], [5], [6]. However, as there are too many current sources with different patterns, it is computationally prohibitive to simulate all possible current waveforms. More importantly, as we have to provide detail current waveforms extracted from the circuit for simulation, such simulation-based algorithms can only be applied when the circuit design is done, while early power grid verification is preferable in practice for ease of grid modification.

To enable early power grid verification, vectorless verification approaches have been proposed [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17]. These approaches use linear current constraints to restrict the feasible set of all possible current waveforms, then solve linear programming (LP) problems to evaluate the worst-case voltage noise. The initial vectorless approach [7] considers the DC analysis model, and it is extended to handle RC and RLC power grids in [8] and [9], respectively. Reference [10] uses an approximate inverse technique to generate a reduced-size LP problem for each node, [11] designs a hierarchical matrix inversion algorithm to compute the inverse of the power grid matrix, [12] and [13] propose convex dual algorithms to solve the LP problem fast. Besides, wavelet analysis is employed in [14] to characterize current excitations in order to identify the worst-case voltage fluctuations. In [15], it is proposed that the VDD network and the GND network should be verified together because their voltage noises have mutual effect through the decoupling capacitors, but this work only consider an RC power grid. Reference [16] introduces hierarchical power constraints for more realistic RLC power grid verification, however, it only verifies the VDD network. Reference [17] proposes a fast approach to compute the bounds of voltage noises in an RLC power grid, but it only considers current constraints within each time step, and doing so may be too pessimistic. Among all these works, only a few consider an RLC power grid as the inductors are difficult to tackle.

In this paper, we consider an integrated RLC power grid model with both VDD and GND networks, and formulate the optimization problems for its vectorless verification. We rigorously prove that the voltage noise at a node, either at a particular time point or cumulatively over a time interval, can be represented as an affine function of current excitations, which enables us to decompose the vectorless verification problem into two orthogonal sub-problems. The first sub-problem is a transient power grid analysis problem that computes the affine function, which can be solved efficiently by existing power grid analysis algorithms. The second sub-problem is a linear programming (LP) problem that maximizes the affine function under a set of current constraints, which can be solved by LP solvers. We introduce transient constraints on current waveforms to restrict them for more realistic scenarios and design the RLCVN (RLC voltage noise) algorithm to evaluate the worst-case voltage noises and identify the corresponding current waveforms at the same time. Experimental results show that the proposed algorithm is effective for RLC power grid verification, and the usage of transient constraints results in more realistic noise prediction.

The rest of this paper is organized as follows. The RLC power grid model and the vectorless verification problem are introduced in Section II. The problem decomposition and the RLCVN algorithm are proposed in Section III. After experimental results are shown in Section IV, we conclude the paper in Section V.

II. RLC Power Grid Verification

A. RLC Power Grid Model

In this paper, we consider an integrated RLC power grid as illustrated in Fig. 1. It consists of resistors, inductors, capacitors, current sources, VDD and GND pads. Each branch is represented by either a resistor, or an inductor, or a capacitor. As this grid has both VDD and GND networks, we refer to the

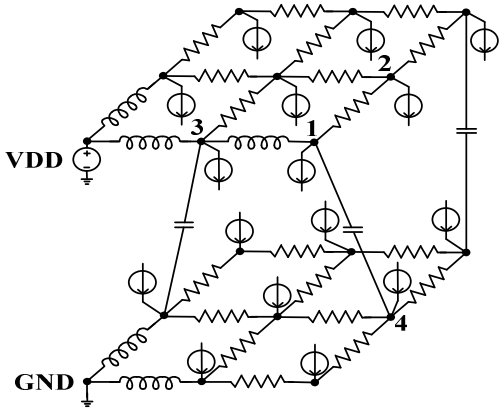

Fig. 1. The RLC power grid model.

nodes in the VDD network as *supply nodes*, and the nodes in the GND network as *ground nodes*. Resistors and inductors are only located between two supply nodes or two ground nodes, while capacitors are only located between a supply node and a ground node. For simplicity of illustration, Fig. 1 only shows at most a single capacitor connected with a node. However, in this paper, we assume that a node can be connected with multiple capacitors. In the VDD network, some supply nodes have ideal current sources representing the currents drawn by the circuitry. Correspondingly, in the GND network, some ground nodes have ideal current sources flowing into them. These current sources model the behavior of the underlying circuitry, which draws current from the VDD network and passes current to the GND network.

Let n be the total number of nodes that are not VDD/GND pads in the power grid, then the goal of grid verification is to evaluate the voltage noise at these non-VDD/GND nodes. Let $u_j(t)$ and $I_j(t)$ be the nodal voltage and the current source at node $j = 1, 2, 3, \cdots, n$, respectively. The positive direction of current is from VDD to GND. The system equations of the power grid can be obtained by applying Kirchoff's Current Law (KCL) at every node j.

For example, applying KCL for node 1 in Fig. 1 leads to

$$g_{1,2}\big(u_1(t) - u_2(t)\big) + i_{1,3}(t) + c_{1,4}\big(u_1(t) - u_4(t)\big)' = -I_1(t),$$
$$u_1(t) - u_3(t) = \ell_{1,3}\big(i_{1,3}(t)\big)',$$

where $g_{1,2}$ is the conductance between node 1 and 2, $i_{1,3}(t)$ is the branch current from node 1 to 3, $c_{1,4}$ is the capacitance between node 1 and 4, $\ell_{1,3}$ is the inductance between node 1 and 3. Rearranging the first equation as an expression of $i_{1,3}(t)$, and then applying that expression to the second equation to cancel $i_{1,3}(t)$, we get

$$u_1(t) - u_3(t) = \ell_{1,3}\Big(- I_1(t) - g_{1,2}\big(u_1(t) - u_2(t)\big) - c_{1,4}\big(u_1(t) - u_4(t)\big)'\Big)'.$$

Rearranging this equation, we have

$$\frac{1}{\ell_{1,3}}\big(u_1(t) - u_3(t)\big) + g_{1,2}\big(u_1(t) - u_2(t)\big)' + c_{1,4}\big(u_1(t) - u_4(t)\big)'' = \big(- I_1(t)\big)'. \quad (1)$$

Let $\mathbf{u}(t)$ and $\mathbf{I}(t)$ be the $n \times 1$ vector of nodal voltages and current sources at these non-VDD/GND nodes, respectively. Let $\mathbf{G}$ be the $n \times n$ conductance matrix, $\mathbf{M}$ be the $n \times n$ matrix similar to the conductance matrix but representing inductance links with its elements being $\frac{1}{\ell}$, $\mathbf{G}_0$ and $\mathbf{M}_0$ be the $n \times n$ matrix representing the conductance and inductance links between these nodes and VDD pads, respectively, and $\mathbf{C}$ be the $n \times n$ matrix similar to the conductance matrix but representing capacitance links. Applying KCL at every non-VDD/GND node j to formulate (1), we have

$$\mathbf{M}\mathbf{u}(t) - \mathbf{M}_0\mathbf{v_{dd}} + \big(\mathbf{G}\mathbf{u}(t) - \mathbf{G}_0\mathbf{v_{dd}}\big)' + \mathbf{C}\mathbf{u}''(t) = \big(\widehat{\mathbf{I}}(t)\big)', \quad (2)$$

where $\mathbf{v_{dd}}$ is a vector whose elements are equal to the supply voltage v_{dd}, and $\widehat{\mathbf{I}}(t)$ is an $n \times 1$ vector representing the incoming current of each node. Its j'th element $\widehat{I}_j(t)$ is defined as

$$\widehat{I}_j(t) \triangleq \begin{cases} -I_j(t), & \text{if node } j \text{ is a supply node,} \\ I_j(t), & \text{if node } j \text{ is a ground node.} \end{cases} \quad (3)$$

In this paper, we assume a single supply voltage, while this RLC power grid model is also applicable for power grids with multiple supply voltages.

B. Simplification of System Equation

Let $\mathbf{v}(t)$ be an $n \times 1$ vector, and define its j'th element $v_j(t)$ as

$$v_j(t) \triangleq \begin{cases} u_j(t) - vdd, & \text{if node } j \text{ is a supply node,} \\ u_j(t), & \text{if node } j \text{ is a ground node.} \end{cases}$$

Obviously, $\mathbf{v}(t)$ is the vector of voltage noises, $\mathbf{v}'(t) = \mathbf{u}'(t)$ and $\mathbf{v}''(t) = \mathbf{u}''(t)$. Since there is no inductors between supply nodes and ground nodes, we have $\mathbf{M}\mathbf{v}(t) = \mathbf{M}\mathbf{u}(t) - \mathbf{M}_0\mathbf{v_{dd}}$. Substituting $\mathbf{v}(t)$ for $\mathbf{u}(t)$ in (2), we obtain

$$\mathbf{M}\mathbf{v}(t) + \mathbf{G}\mathbf{v}'(t) + \mathbf{C}\mathbf{v}''(t) = \big(\widehat{\mathbf{I}}(t)\big)', \quad (4)$$

where the constant vector $\mathbf{G}_0\mathbf{v_{dd}}$ is dropped because of the differential operation. Using the backward Euler method, (4) can be discretized in time and rearranged as

$$\Big(\mathbf{G} + \mathbf{M}\Delta t + \frac{\mathbf{C}}{\Delta t}\Big)\mathbf{v}(t) = \widehat{\mathbf{I}}(t) - \widehat{\mathbf{I}}(t - \Delta t) + \Big(\mathbf{G} + \frac{2\mathbf{C}}{\Delta t}\Big)\mathbf{v}(t - \Delta t) - \frac{\mathbf{C}}{\Delta t}\mathbf{v}(t - 2\Delta t), \quad (5)$$

where Δt is the time step. Clearly, the system equation (5) is similar to the DC analysis equation, where the left-hand-side power grid matrix is a combination of R/L/C components, and the right-hand-side vector is computed from current and previous $\widehat{\mathbf{I}}/\mathbf{v}$ states.

For simplicity of notations, we define $n \times n$ matrix $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{G}_{\mathrm{C}}$ as

$$\mathbf{A} \triangleq \mathbf{G} + \mathbf{M}\Delta t + \frac{\mathbf{C}}{\Delta t},\ \mathbf{B} \triangleq \mathbf{G} + \frac{2\mathbf{C}}{\Delta t},\ \mathbf{G}_{\mathrm{C}} \triangleq \frac{\mathbf{C}}{\Delta t}.$$

Note that $\mathbf{A}$ is a symmetric $\mathbf{M}$-matrix, while $\mathbf{B}$ and $\mathbf{G}_{\mathrm{C}}$ are also symmetric. Therefore, $\mathbf{A}$ is invertible and $\mathbf{A}^{-1}$ is symmetric. Equation (5) can be simplified and rearranged as

$$\mathbf{v}(t) = \mathbf{A}^{-1}\big(\widehat{\mathbf{I}}(t) - \widehat{\mathbf{I}}(t - \Delta t) + \mathbf{B}\mathbf{v}(t - \Delta t) - \mathbf{G}_{\mathrm{C}}\mathbf{v}(t - 2\Delta t)\big). \quad (6)$$

Now, (6) represents the voltage noises at time t as a function of current excitations and the voltage noises at previous time steps. It will be used to verify the voltage noise across the power grid.

C. Current Constraints

To capture the infinite many current waveforms in the power grid, we employ the framework of current constraints. As studied in [15], the current waveforms of the power grid including both VDD and GND networks can be modeled by three types of constraints: *local constraints*, *global constraints* and *equality constraints*.

Since the maximum value of each current source is usually bounded, local constraints are introduced to define an upper bound for individual current source,

$$0 \le \mathbf{I}(t) \le \mathbf{I}_L, \forall t, \text{ or } 0 \le \mathbf{I}(k\Delta t) \le \mathbf{I}_L, \forall k,$$

where $\mathbf{I}_L \ge 0$ is an $n \times 1$ upper bound vector. In practice, it is never the case that all the gates or cells draw their peak currents simultaneously. Therefore, global constraints are introduced to define upper bounds for groups of current sources.

$$\mathbf{UI}(t) \le \mathbf{I}_G, \forall t, \text{ or } \mathbf{UI}(k\Delta t) \le \mathbf{I}_G, \forall k,$$

Let m be the number of global constraints, then U is an $m \times n$ $0/1$ matrix indicating the assignments of current sources to groups, and $\mathbf{I}_G \ge 0$ is an $m \times 1$ upper bound vector.

To verify both VDD and GND networks, we must ensure that the current flowing out of the VDD network is equal to the current flowing into the GND network. For a circuit block, this is also true if the input and output currents are negligible. Equality constraints are introduced to model this relationship. If we assume that there are b circuit blocks satisfying this equality relationship, then the equality constraints can be formulated as:

$$\mathbf{EI}(t) = 0, \forall t, \text{ or } \mathbf{EI}(k\Delta t) = 0, \forall k,$$

where $\mathbf{E}$ is a $b \times n$ matrix consisting of ± 1s and 0s. For each circuit block, $+1$s and -1s correspond to the current sources that are attached to the VDD and GND network, respectively, while 0s correspond to other current sources.

The current excitations at a particular time t is well defined by these three types of current constraints. However, these constraints can not model the transient behavior of current sources. When verifying the power grid, ignoring the transient behavior will lead to pessimistic estimation of the voltage noise, which is caused by un-realistic transient waveforms. For example, the node connected with a gate would have maximum voltage noise when the gate always draws the maximum current, which is never the case.

In order to capture the transient behavior of current sources, we propose novel *transient constraints* to restrict the total amount of current (or more exactly "charge") that each current source can draw within a time interval, i.e. a number of continuous time steps. Let N_{ts} be the number of time steps under consideration, then transient constraints can be formulated as

$$\int_0^{N_{ts} \times \Delta t} \mathbf{I}(t)dt \le \mathbf{I}_T \times \Delta t, \text{ or } \sum_{k=1}^{N_{ts}} \mathbf{I}(k\Delta t) \le \mathbf{I}_T,$$

where $\mathbf{I}_T \ge 0$ is an $n \times 1$ upper bound vector, and the integration operation is element-wise. To extract these transient constraints from the underlying circuitry, we must analyze the circuit to derive the maximum amount of switching instants for each gate/cell within N_{ts} time steps, then translate these switching instants into current waveforms, and finally discretize the waveform to get transient upper bounds. As switching activity analysis has already been studied in [18] and [19], we can follow these works to compute $\mathbf{I}_T$.

Except for the afore-mentioned constraints, some other constraints have also been proposed to characterize current waveforms. In [14], the authors introduce *max delta constraints* to bound the change in current between successive time units. Moreover, reference [20] uses *current slope constraints* to bound the minimum current transition time. Both of these constraints restrict the transition characteristics of current sources. In addition, *power constraints* are proposed in [16] to bound the power consumption of circuit blocks. In practice, we may need a combination of different types of constraints to characterize the feasible current excitations for vectorless power grid verification. However, in this paper, we only consider local constraints, global constraints, equality constraints, and transient constraints, while the proposed vectorless verification approach can also be extended to handle other constraints.

D. Problem Formulation

As studied in [9] and [15], the nodal voltage of an RLC/RC power grid can fluctuate in both directions, i.e. overshot and voltage drop in the VDD network, ground bounce and undershot in the GND network. In order to obtain the worst-case voltage noise at each node, we need to evaluate the voltage noise in both directions.

Assume that there is no current excitation for all $t \le 0$, so that $\mathbf{v}(t) = 0$, $\forall t \le 0$. Consider N_{ts} time steps, then the vectorless verification is to solve the following optimization problem for every node $1 \le j \le n$,

$$\begin{aligned} &\text{Maximize/Minimize } v_j(t), \ \forall t = k'\Delta t, 1 \le k' \le N_{ts}, \qquad (7)\\ &\text{subject to: } \forall 1 \le k \le N_{ts}, \mathbf{v}(k\Delta t) = \mathbf{A}^{-1}\Big(\widehat{\mathbf{I}}(k\Delta t) - \widehat{\mathbf{I}}\big((k-1)\Delta t\big) + \\ &\qquad \mathbf{B}\mathbf{v}\big((k-1)\Delta t\big) - \mathbf{G}_C\mathbf{v}\big((k-2)\Delta t\big)\Big), \\ &0 \le \mathbf{I}(k\Delta t) \le \mathbf{I}_L, \mathbf{UI}(k\Delta t) \le \mathbf{I}_G, \mathbf{EI}(k\Delta t) = 0, \sum_{k=1}^{N_{ts}} \mathbf{I}(k\Delta t) \le \mathbf{I}_T, \end{aligned}$$

where $\widehat{\mathbf{I}}(t)$ is defined in (3), and it represents the incoming current of each node. By maximizing the voltage noise, we get the worst-case overshot or ground bounce. By minimizing the voltage noise, we obtain the worst-case voltage drop or undershot. Clearly, two linear programming (LP) problems need to be solved for each node at each time step. Note that there is a group of constraints for each time step except for the transient constraints, resulting in potentially very complicate problems.

According to [9], the optimization problems at time $t - \Delta t$ are sub-problems of the optimization problems at time t. For each node, the magnitude of the worst-case voltage noise is a non-decreasing function for all $t \ge 0$, and this is also proved in [16]. Therefore, we only need to solve two LP problems for each node at time $t = N_{ts}\Delta t$ to verify the grid. For every node $1 \le j \le n$,

$$\begin{aligned} &\text{Maximize/Minimize } v_j(N_{ts}\Delta t), \qquad (8)\\ &\text{subject to the same set of constraints as stated in (7).} \end{aligned}$$

Although most works are focusing on solving the worst-case voltage noise at each node, it is proposed in [21] that verifying the integral of voltage noise (or the mean voltage noise) is more important, because a sharp voltage noise may not affect timing, but a large cumulative voltage noise will. Let's still consider N_{ts} time steps, then the problem for verifying the integral of voltage noise can be formulated as follows. For every node $1 \le j \le n$,

$$\begin{aligned} &\text{Maximize/Minimize } \sum_{k'=1}^{N_{ts}} v_j(k'\Delta t), \qquad (9)\\ &\text{subject to the same set of constraints as stated in (7).} \end{aligned}$$

However, it is very challenging to solve either (8) or (9) directly, because the constraints are too complicated, especially the relationships between voltage noises and current

excitations. As there are $2n$ LP problems and n is usually large for practical power grids, such LP problems have to be solved very efficiently.

III. Proposed Approach

In this Section, we first introduce two important properties of the system equation in Section III-A, formulate the expression of nodal voltages in Section III-B, then present the problem decomposition in Section III-C, and finally propose the RLCVN algorithm in Section III-D.

A. Properties of System Equation

Based on the initial condition that the power grid has no stimulus when $t \leq 0$, we can write the system equation of the power grid at different time steps according to (6). At time $t = \Delta t, 2\Delta t,$ and $3\Delta t$, we have

$$\begin{aligned}
\mathbf{v}(\Delta t) &= \mathbf{A}^{-1}\widehat{\mathbf{I}}(\Delta t) \\
\mathbf{v}(2\Delta t) &= \mathbf{A}^{-1}\left(\widehat{\mathbf{I}}(2\Delta t) - \widehat{\mathbf{I}}(\Delta t) + \mathbf{B}\mathbf{v}(\Delta t)\right) \\
&= \mathbf{A}^{-1}\widehat{\mathbf{I}}(2\Delta t) + \mathbf{A}^{-1}\left(\mathbf{B}\mathbf{A}^{-1} - \mathbb{I}_n\right)\widehat{\mathbf{I}}(\Delta t) \\
\mathbf{v}(3\Delta t) &= \mathbf{A}^{-1}\left(\widehat{\mathbf{I}}(3\Delta t) - \widehat{\mathbf{I}}(2\Delta t) + \mathbf{B}\mathbf{v}(2\Delta t) - \mathbf{G}_{\mathrm{C}}\mathbf{v}(\Delta t)\right) \\
&= \mathbf{A}^{-1}\widehat{\mathbf{I}}(3\Delta t) + \mathbf{A}^{-1}(\mathbf{B}\mathbf{A}^{-1} - \mathbb{I}_n)\widehat{\mathbf{I}}(2\Delta t) \\
&\quad + \mathbf{A}^{-1}\left(\mathbf{B}\mathbf{A}^{-1}(\mathbf{B}\mathbf{A}^{-1} - \mathbb{I}_n) - \mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}\right)\widehat{\mathbf{I}}(\Delta t)
\end{aligned}$$

where $\mathbb{I}_n$ is an $n \times n$ identity matrix.

Lemma 1: There exist a unique series of $n \times n$ matrices $\mathbf{S}_1, \mathbf{S}_2, \cdots, \mathbf{S}_k, \mathbf{S}_{k+1}, \cdots$, such that $\forall k \geq 1$, we have

$$\mathbf{v}(k\Delta t) = \mathbf{S}_1\widehat{\mathbf{I}}(k\Delta t) + \mathbf{S}_2\widehat{\mathbf{I}}((k-1)\Delta t) + \cdots + \mathbf{S}_k\widehat{\mathbf{I}}(\Delta t). \tag{10}$$

Proof: According to the expression of $\mathbf{v}(\Delta t)$ and $\mathbf{v}(2\Delta t)$, we have

$$\mathbf{S}_1 = \mathbf{A}^{-1}, \mathbf{S}_2 = \mathbf{A}^{-1}(\mathbf{B}\mathbf{A}^{-1} - \mathbb{I}_n). \tag{11}$$

Based on the expression of $\mathbf{v}(3\Delta t)$ and (6), we can infer that

$$\mathbf{S}_k = \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_{k-1} - \mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2}), \forall k \geq 3. \tag{12}$$

Lemma 1 and 12 can be proved by induction as follows.

Obviously, Lemma 1, (11) and (12) are true when $k = 1, 2, 3$. For $k \geq 4$, assume that

$$\begin{aligned}
\mathbf{v}_{k-2} &= \mathbf{S}_1\widehat{\mathbf{I}}_{k-2} + \mathbf{S}_2\widehat{\mathbf{I}}_{k-3} + \cdots + \mathbf{S}_{k-2}\widehat{\mathbf{I}}_1, \\
\mathbf{v}_{k-1} &= \mathbf{S}_1\widehat{\mathbf{I}}_{k-1} + \mathbf{S}_2\widehat{\mathbf{I}}_{k-2} + \cdots + \mathbf{S}_{k-1}\widehat{\mathbf{I}}_1,
\end{aligned}$$

where $\mathbf{v}_k$ and $\widehat{\mathbf{I}}_k$ represent $\mathbf{v}(k\Delta t)$ and $\widehat{\mathbf{I}}(k\Delta t)$, respectively. Also assume that (11) is true, and $\mathbf{S}_j = \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_{j-1} - \mathbf{G}_{\mathrm{C}}\mathbf{S}_{j-2})$, $\forall 3 \leq j \leq k-1$. Then, according to (6), we have

$$\begin{aligned}
\mathbf{v}_k &= \mathbf{A}^{-1}(\widehat{\mathbf{I}}_k - \widehat{\mathbf{I}}_{k-1} + \mathbf{B}\mathbf{v}_{k-1} - \mathbf{G}_{\mathrm{C}}\mathbf{v}_{k-2}) \\
&= \mathbf{A}^{-1}\widehat{\mathbf{I}}_k + \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_1 - \mathbb{I}_n)\widehat{\mathbf{I}}_{k-1} + \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_2 - \\
&\quad \mathbf{G}_{\mathrm{C}}\mathbf{S}_1)\widehat{\mathbf{I}}_{k-2} + \cdots + \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_{k-2} - \mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-3})\widehat{\mathbf{I}}_2 + \\
&\quad \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_{k-1} - \mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2})\widehat{\mathbf{I}}_1 \\
&= \mathbf{S}_1\widehat{\mathbf{I}}_k + \mathbf{S}_2\widehat{\mathbf{I}}_{k-1} + \cdots + \mathbf{S}_{k-1}\widehat{\mathbf{I}}_2 + \mathbf{S}_k\widehat{\mathbf{I}}_1,
\end{aligned}$$

where (11) still holds, and $\mathbf{S}_j = \mathbf{A}^{-1}(\mathbf{B}\mathbf{S}_{j-1} - \mathbf{G}_{\mathrm{C}}\mathbf{S}_{j-2})$, $\forall 3 \leq j \leq k$. Therefore, by induction, Lemma 1 is true, and S_k satisfies (11) and (12). ■

Lemma 2: $\forall k \geq 1$, $\mathbf{S}_k$ is symmetric.

Proof: Recall that $\mathbf{A}^{-1}$, $\mathbf{B}$ and $\mathbf{G}_{\mathrm{C}}$ are symmetric. So $\mathbf{S}_1 = \mathbf{A}^{-1}$ is symmetric, and $\mathbf{S}_2 = \mathbf{A}^{-1}(\mathbf{B}\mathbf{A}^{-1} - \mathbb{I}_n) = \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1} - \mathbf{A}^{-1}$ is also symmetric due to the fact that $\mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}$ is symmetric. Similarly, we can verify that $\mathbf{S}_3$ is symmetric. Besides, we observe that $\forall k \geq 2$,

$$\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_k - \mathbf{S}_k\mathbf{B}\mathbf{A}^{-1} = \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-1} - \mathbf{S}_{k-1}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}. \tag{13}$$

Lemma 2 and (13) can be proved by induction as follows.

It can be verified that (13) holds when $k = 2, 3$. For $k \geq 4$, assume that $\mathbf{S}_{k-3}$, $\mathbf{S}_{k-2}$ and $\mathbf{S}_{k-1}$ are symmetric, and

$$\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-1} - \mathbf{S}_{k-1}\mathbf{B}\mathbf{A}^{-1} = \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2} - \mathbf{S}_{k-2}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}. \tag{14}$$

According to (12) and this assumption, we have

$$\begin{aligned}
\mathbf{S}_k &= \mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-1} - \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2} \\
\mathbf{S}_k^T &= \mathbf{S}_{k-1}^T\mathbf{B}^T(\mathbf{A}^{-1})^T - \mathbf{S}_{k-2}^T\mathbf{G}_{\mathrm{C}}^T(\mathbf{A}^{-1})^T \\
&= \mathbf{S}_{k-1}\mathbf{B}\mathbf{A}^{-1} - \mathbf{S}_{k-2}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1} = \mathbf{S}_k.
\end{aligned}$$

So $\mathbf{S}_k$ is also symmetric, and

$$\begin{aligned}
&\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_k - \mathbf{S}_k\mathbf{B}\mathbf{A}^{-1} \\
&= \mathbf{A}^{-1}\mathbf{B}(\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-1} - \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2}) - \\
&\quad (\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-1} - \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2})\mathbf{B}\mathbf{A}^{-1} \\
&= \mathbf{A}^{-1}\mathbf{B}(\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-1} - \mathbf{S}_{k-1}\mathbf{B}\mathbf{A}^{-1}) - \\
&\quad \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2} + \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2}\mathbf{B}\mathbf{A}^{-1} \\
&= \mathbf{A}^{-1}\mathbf{B}(\mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2} - \mathbf{S}_{k-2}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}) - \\
&\quad \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2} + \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2}\mathbf{B}\mathbf{A}^{-1} \\
&= \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2}\mathbf{B}\mathbf{A}^{-1} - \mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-2}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}.
\end{aligned} \tag{15}$$

Recall that $\mathbf{S}_{k-3}$, $\mathbf{S}_{k-2}$ and $\mathbf{S}_{k-1}$ are symmetric due to the assumption. So

$$\begin{aligned}
\mathbf{S}_{k-1} &= \mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-2} - \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-3} = \mathbf{S}_{k-1}^T \\
&= \mathbf{S}_{k-2}\mathbf{B}\mathbf{A}^{-1} - \mathbf{S}_{k-3}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1},
\end{aligned}$$

and then,

$$\begin{aligned}
&\mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-1} - \mathbf{S}_{k-1}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1} \\
&= \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}(\mathbf{S}_{k-2}\mathbf{B}\mathbf{A}^{-1} - \mathbf{S}_{k-3}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}) - \\
&\quad (\mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-2} - \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-3})\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1} \\
&= \mathbf{A}^{-1}\mathbf{G}_{\mathrm{C}}\mathbf{S}_{k-2}\mathbf{B}\mathbf{A}^{-1} - \mathbf{A}^{-1}\mathbf{B}\mathbf{S}_{k-2}\mathbf{G}_{\mathrm{C}}\mathbf{A}^{-1}.
\end{aligned} \tag{16}$$

Combining (15) and (16), we get equation (13), and then we can further prove that $\mathbf{S}_{k+1}$ is symmetric. Therefore, by induction, (13) must hold and Lemma 2 is true. ■

B. Voltage Noise at Each Node

Let $\mathbf{e}_j$ be an $n \times 1$ vector of all 0's except the j'th component being 1. Assume that $\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j$, and $\widehat{\mathbf{I}}(p\Delta t) = 0$, $\forall 2 \leq p \leq k$. Define $\mathbf{c}_{j,k}$ as the vector of corresponding voltage noises at time $t = k\Delta t$, $\forall k \geq 1$. According to (10), we get

$$\mathbf{c}_{j,k} \triangleq \mathbf{v}(k\Delta t) \mid_{\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j, \widehat{\mathbf{I}}(p\Delta t) = 0, \forall 2 \leq p \leq k} = \mathbf{S}_k\mathbf{e}_j. \tag{17}$$

Note that $\mathbf{c}_{j,k}$ is the j'th column of $\mathbf{S}_k$. As $\mathbf{S}_k$ is symmetric, its j'th row is equal to $\mathbf{c}_{j,k}^T$. Applying this fact to (10), we can write the voltage noise of each node $1 \leq j \leq n$ at time $t = k\Delta t, \forall k \geq 1$ as

$$v_j(k\Delta t) = \mathbf{c}_{j,1}^T\widehat{\mathbf{I}}(k\Delta t) + \mathbf{c}_{j,2}^T\widehat{\mathbf{I}}((k-1)\Delta t) + \cdots + \mathbf{c}_{j,k}^T\widehat{\mathbf{I}}(\Delta t), \tag{18}$$

where the voltage noise is represented as a linear function of current excitations at different time steps.

Consider the power grid as an n-input-n-output linear system with input current vector $\widehat{\mathbf{I}}(t)$ and output voltage noise vector $\mathbf{v}(t)$. Conventionally, to represent a particular output as an affine function of inputs for such a linear system, we have to compute the impulse response of each input. However, because of the symmetry of $\mathbf{S}_k$ as stated in Lemma 2, the power grid has symmetric impulse responses. For example, let's consider two nodes j_1 and j_2 shown in Fig. 2. We apply an impulse current excitation at one node, and evaluate the voltage noise response at the other node. These two nodes would have the same response due to symmetry. For each node, its voltage noise responses corresponding to the impulse current excitations at all the nodes are equal to the voltage

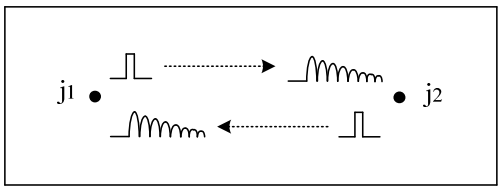

Fig. 2. Symmetric impulse response of two nodes in the power grid.

noise responses of all the nodes corresponding to the impulse current excitation at the node itself. In fact, this symmetry has been employed to represent the voltage noise of each node as an affine function of current sources in (18), where $\mathbf{c}_{j,k}$ is the vector of voltage noise responses of all the nodes at time $t = k\Delta t$ corresponding to the impulse current excitation at node j when $t = \Delta t$. Note that (18) can also be viewed as the convolution of impulse responses and inputs.

C. Problem Decomposition

Applying (18) to represent the voltage noise, we can decompose the optimization problem (8) into the following two sub-problems. For each node $1 \leq j \leq n$,

$$\text{I: Compute } \mathbf{c}_{j,k},\ \forall 1 \leq k \leq N_{ts}, \tag{19}$$

$$\text{II: Maximize/Minimize } v_j(N_{ts}\Delta t) = \sum_{k=1}^{N_{ts}} \mathbf{c}_{j,k}^T \widehat{\mathbf{I}}\big((N_{ts}+1-k)\Delta t\big) \tag{20}$$

$$\text{subject to: } 0 \leq \mathbf{I}(k\Delta t) \leq \mathbf{I}_L, \mathbf{U}\mathbf{I}(k\Delta t) \leq \mathbf{I}_G,$$

$$\mathbf{E}\mathbf{I}(k\Delta t) = 0, \sum_{k=1}^{N_{ts}} \mathbf{I}(k\Delta t) \leq \mathbf{I}_T.$$

According to the definition of $\mathbf{c}_{j,k}$ in (17), the first sub-problem is numerically a power grid analysis problem with an impulse current excitation $\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j$. Different from conventional power gird transient analysis with realistic current waveforms to evaluate voltage noises, here we use impulse current excitation for power grid simulation to characterize voltage noise responses. The second sub-problem is still linear programming (LP) but it is much easier to solve compared to (8), because the voltage noise is formulated as a linear function of current sources. Note that without the transient constraints, the LP problems (20) can be further divided into many smaller LP problems at each time step and solved independently. In comparison with the exact approach of [9], this problem decomposition largely simplifies the vectorless verification of RLC power grids.

D. The RLCVN Algorithm

Using the problem decomposition, we design the RLCVN (RLC voltage noise) algorithm shown in Fig. 3 to solve the vectorless verification problem (8). For each node, we first perform transient simulation with an impulse current excitation to compute $\mathbf{c}_{j,k}, \forall 1 \leq k \leq N_{ts}$, and then solve two LP problems to evaluate the worst-case voltage noises in both directions. As a byproduct of solving the LP problems, the corresponding current waveforms leading to the worst-case voltage noises can also be obtained. Such current waveforms are important for designers as they serve as guidelines for grid modification. Therefore, the proposed algorithm is capable of evaluating worst-case voltage noises and identifying corresponding current waveforms.

The merit of this algorithm is that it verifies each node by two orthogonal phases: power grid transient simulation and

Algorithm RLCVN

Inputs

$\mathbf{G}$, $\mathbf{M}$, $\mathbf{C}$: R/L/C matrices, defined in Section II-A.
$\mathbf{I}_L$, $\mathbf{U}$, $\mathbf{I}_G$, $\mathbf{E}$, $\mathbf{I}_T$: vectors/matrices of constraints, defined in Section II-C.
Δt, N_{ts}: time step, and the number of time steps.

Outputs

Worst-case voltage noises at each node, and the corresponding current waveforms.

1 **For** each node $j = 1$ to n
2 Simulate the power grid for N_{ts} time steps to compute $\mathbf{c}_{j,k}, \forall 1 \leq k \leq N_{ts}$ using an impulse current excitation $\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j$
3 Maximize/minimize equation (20) subject to current constraints to get the worst-case voltage noises in both directions and the corresponding current waveforms

Fig. 3. The RLCVN algorithm.

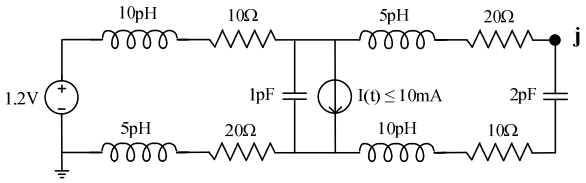

Fig. 4. A simple RLC power grid.

noise optimization. As the left-hand-side matrix of the system equation (5) is a symmetric $\mathbf{M}$-matrix, it represents a resistor network, which can be obtained by converting the inductance and capacitance links into resistance branches accordingly. Then, the RLC power grid is reduced into a pure resistor network, which can be simulated very efficiently by using existing power grid analysis algorithms. In our implementation, we employ the preconditioned conjugate gradient (PCG) method [1], [22] with a random-walk based preconditioner [23] for fast power grid simulation. The noise optimization is based on the framework of current constraints. In fact, the proposed algorithm can be extended to handle other kinds of constraints, such as max delta constraints [14] and power constraints [16].

Besides, the RLCVN algorithm can also be extended to verify the integral of voltage noise (9) without any extra computational overhead. One just needs to replace the impulse current excitation $\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j$ with continuous current value $\widehat{\mathbf{I}}(k\Delta t) = \mathbf{e}_j, \forall 1 \leq k \leq N_{ts}$ for power grid transient simulation. This property can be proved using (17) and (18). Here we omit the proof due to lack of space.

IV. Experimental Results

The RLCVN algorithm is implemented in C++, and the LP problems (20) for noise optimization are solved by MOSEK [24]. In this Section, we first use a case study to show the effectiveness of the proposed algorithm, and then present the performance results using synthetic power grids.

A. A Case Study

Consider the simple RLC power grid shown in Fig. 4. We employ the RLCVN algorithm to verify node **j** using time step $\Delta t = 10$ps and the number of time steps $N_{ts} = 100$.

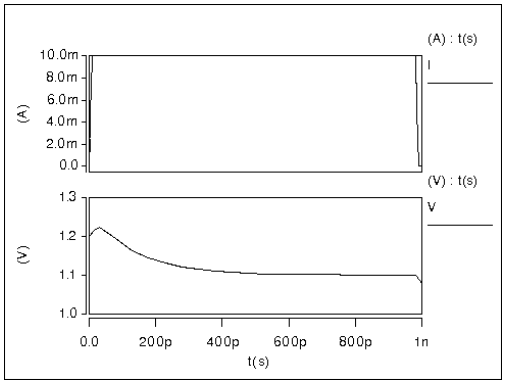

Fig. 5. HSPICE simulation waveforms of the current source and the voltage at node **j**, where node **j** has the maximum voltage drop of 118.4mV at $t = 1$ns without a transient constraint.

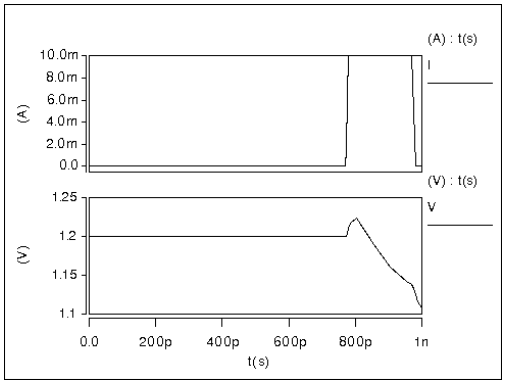

Fig. 6. HSPICE simulation waveforms of the current source and the voltage at node **j**, where node **j** has the maximum voltage drop of 86.5mV at $t = 1$ns with a transient constraint $\sum_{k=1}^{100} I(k \times 10\text{ps}) \leq 200$mA.

In other words, we evaluate the worst-case voltage noise of node **j** at $t = 1$ns with a zero initial condition. Note that the worst-case voltage noise at $t = 1$ns is the worst-case voltage noise from $t = 0$ to 1ns as discussed in Section II-D. Without a transient constraint for the current source, the worst-case voltage drop is 118.4mV, which is caused by a consistent current of 10mA from 10ps to 980ps. If we specify a transient constraint $\sum_{k=1}^{100} I(k \times 10\text{ps}) \leq 200$mA to restrict the current waveform, then the worst-case voltage drop is 86.5mV, which is caused by a consistent current of 10mA from 780ps to 970ps. Fig. 5 and 6 show the HSPICE simulation waveforms of these two cases, respectively. Clearly, without the transient constraint, the worst-case voltage noise is more pessimistic. From Fig. 5 and 6, we can observe that node **j** has overshots. Using the RLCVN algorithm, we are able to obtain that the worst-case overshot at $t = 1$ns is 18.5mV, which is due to a 10mA current from 990ps to 1ns. The corresponding HSPICE simulation waveforms are illustrated in Fig. 7. For this particular node, the worst-case overshots with/without the transient constraint are the same, because the corresponding current waveform satisfies the devised transient constraint.

In summary, the RLCVN algorithm solves the worst-case voltage noises and identifies the corresponding current waveforms, which are realistic but nonobvious to designers. The effectiveness of the RLCVN algorithm is also confirmed by corresponding HSPICE simulation results.

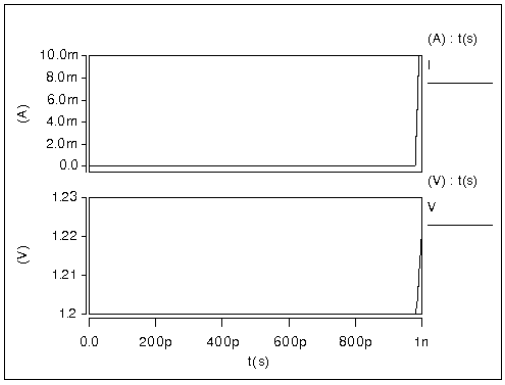

Fig. 7. HSPICE simulation waveforms of the current source and the voltage at node **j**, where node **j** has the maximum overshot of 18.5mV at $t = 1$ns.

TABLE I
AVERAGE RUNTIME PER NODE OF THE RLCVN ALGORITHM

Power Grids	Nodes	Current Sources	Simulation Runtime	LP Runtime	
				Simplex	Interior Point
RLC_pg100	176	72	0.005 s	0.36 s	0.40 s
RLC_pg200	568	242	0.025 s	1.92 s	1.98 s
RLC_pg300	1184	512	0.063 s	6.89 s	6.13 s
RLC_pg400	2024	882	0.126 s	15.60 s	12.70 s
RLC_pg500	3088	1352	0.180 s	48.62 s	30.97 s
RLC_pg1000	11768	5202	0.769 s	6.36 min	7.32 min

B. Performance Results

To evaluate the performance of the RLCVN algorithm, we generate 6 RLC power grids with 4 metal layers, 1.2V VDD, and various C4 bumps/chip sizes/power consumptions. The pad inductances are set to 10pH, and the decoupling capacitances are set to 40pF. Note that these power grids have both VDD and GND networks as shown in Fig. 1. For each power grid, we extract local constraints from the grid description, generate equality and transient constraints, and specify up to 10 global constraints hierarchically. All experiments are carried out on a 64-bit Linux server with 2.4GHz Intel Q6600 processor and 8GB memory. Although the processor has multiple cores, only a single core is used for experiments.

We apply the RLCVN algorithm to verify these synthetic power grids using time step $\Delta t = 10$ps and the number of time steps $N_{ts} = 100$. Table I shows the average runtime per node. The runtime can be generally partitioned into two parts: the runtime for power gird transient simulation, and the runtime to solve the LP problems for noise optimization. These two parts are reported under the column "Simulation Runtime" and "LP Runtime", respectively. Since MOSEK provides both the simplex method and the interior point method to solve LP problems, we experiment with both options and their results are reported under the column "simplex" and "interior point", respectively. For the largest power grid "RLC_pg1000", the reported runtime is an estimation from 100 random nodes. Clearly, the power grid simulation time is very small as the random-walk based PCG method is fairly efficient. Most of the runtime is spent on solving the LP problems, and the LP runtime increases quadratically as the size of the power grid increases.

To demonstrate that omitting transient constraints may result in pessimistic voltage noise prediction, we perform experiments without transient constraints for comparison. Table II

TABLE II
WORST-CASE VOLTAGE NOISES OF A RANDOM NODE WITH AND WITHOUT TRANSIENT CONSTRAINTS

Power Grids	Node Type	Without Transient Constraints		With Transient Constraints		Overestimation	
		overshot/ground bounce (mV)	voltage drop/ undershot (mV)	overshot/ground bounce (mV)	voltage drop/ undershot (mV)	overshot/ground bounce	voltage drop/ undershot
RLC_pg100	supply	0.63	8.94	0.63	4.81	0.00%	85.80%
RLC_pg200	ground	32.91	6.49	14.29	6.49	130.35%	0.00%
RLC_pg300	supply	4.47	23.85	4.47	12.45	0.00%	91.57%
RLC_pg400	ground	47.65	16.39	27.04	16.39	76.25%	0.00%
RLC_pg500	supply	22.57	43.55	22.53	31.18	0.14%	39.66%
RLC_pg1000	ground	31.86	19.76	23.06	19.68	38.17%	0.42%

shows the worst-case voltage noises of a random node with and without transient constraints. Note that each node has two worst-case voltage noises, i.e. overshot/voltage drop of a supply node, ground bounce/undershot of a ground node. An interesting phenomenon is that omitting transient constraints leads to significant percentage of overestimation for the voltage drop of a supply node and the ground bounce of a ground node, while it has minor impact on overshots and undershots. This phenomenon would be attributable to the fact that overshots and undershots are usually caused by sharp current switching activities, which are not restricted by transient constraints. Generally, with transient constraints, we can get more realistic voltage noise estimations, thus avoiding costly overdesigns of the power grid.

In conclusion, the RLCVN algorithm can be applied for vectorless verification of practical RLC power grids. One might complain that the synthetic power grids are small, and the per node runtime is large. However, our algorithm is important for at least three reasons. First, the size of the RLC power grid model is dependent on the level of model extraction. In practice, our algorithm can be applied either to parts of the power grid, or to the top-level network of the grid. Second, our algorithm can be easily paralleled as each node is verified independently. Third, as discussed in [16], one can apply our algorithm to verify a few risky nodes of the grid. Therefore, we believe that the RLCVN algorithm is a practical method for RLC power gird verification.

V. CONCLUSION

In this paper, we studied the vectorless verification of power grids using an integrated RLC power grid model. Our study showed that the vectorless verification of RLC power grids can be divided into two phases: power grid transient simulation and noise maximization. We proposed transient constraints to restrict the waveform of each current source, such that the worst-case voltage noise estimations can be more realistic. Moreover, we designed the RLCVN algorithm for vectorless verification of RLC power grids. Experimental results confirmed that it is an effective approach for computing the worst-case voltage noises and identifying the corresponding current excitations. We also observed that verifying power grids with transient constraints is much slower compared to solving optimization problems at individual time step without transient constraints. Future work would be to explore efficient algorithms to solve the LP problem (20).

REFERENCES

[1] T.-H. Chen and C. C.-P. Chen, "Efficient large-scale power grid analysis based on preconditioned Krylov-subspace iterative methods," in *Proc. Design Automation Conf. (DAC)*, 2001, pp. 559–562.

[2] J. N. Kozhaya, S. R. Nassif, and F. N. Najm, "A multigrid-like technique for power grid analysis," *IEEE Trans. Computer-Aided Design*, vol. 21, issue 10, pp. 1148–1160, Oct. 2002.

[3] M. Zhao, R. V. Panda, S. S. Sapatnekar, and D. Blaauw, "Hierarchical analysis of power distribution networks," *IEEE Trans. Computer-Aided Design*, vol. 21, no. 2, pp. 159–168, Feb. 2002.

[4] Y.-M. Lee, Y. Cao, T.-H. Chen, J. M. Wang, and C. C.-P. Chen, "HiPRIME: hierarchical and passivity preserved interconnect macromodeling engine for RLKC power delivery," *IEEE Trans. Computer-Aided Design*, vol. 24, no. 6, pp. 797–806, Jun. 2005.

[5] H. Qian, S. R. Nassif, and S. S. Sapatnekar, "Power grid analysis using random walks," *IEEE Trans. Computer-Aided Design*, vol. 24, no. 8, pp. 1204–1224, Aug. 2005.

[6] X. Hu, W. Zhao, P. Du, A. Shayan, and C.-K. Cheng, "An adaptive parallel flow for power distribution network simulation using discrete Fourier transform," in *Proc. Asia and South Pacific Design Automation Conf. (ASPDAC)*, 2010, pp. 125–130.

[7] D. Kouroussis and F. N. Najm, "A static pattern-independent technique for power grid voltage integrity verification," in *Proc. Design Automation Conf. (DAC)*, 2003, pp. 99–104.

[8] I. A. Ferzli, F. N. Najm, and L. Kruse, "A geometric approach for early power grid verification using current constraints," in *Proc. Int. Conf. Computer-Aided Design (ICCAD)*, 2007, pp. 40–47.

[9] N. H. Abdul Ghani and F. N. Najm, "Handling inductance in early power grid verification," in *Proc. Int. Conf. Computer-Aided Design (ICCAD)*, 2006, pp. 127–134.

[10] N. H. Abdul Ghani and F. N. Najm, "Fast vectorless power grid verification using an approximate inverse technique," in *Proc. Design Automation Conf. (DAC)*, 2009, pp. 184–189.

[11] X. Xiong and J. Wang, "A hierarchical matrix inversion algorithm for vectorless power grid verification," in *Proc. Int. Conf. Computer-Aided Design (ICCAD)*, 2010, pp. 543–550.

[12] X. Xiong and J. Wang, "An efficient dual algorithm for vectorless power grid verification under linear current constraints," in *Proc. Design Automation Conf. (DAC)*, 2010, pp. 837–842.

[13] X. Xiong and J. Wang, "Dual algorithms for vectorless power grid verification under linear current constraints," *IEEE Trans. Computer-Aided Design*, 2011, to appear.

[14] I. A. Ferzli, E. Chiprout, and F. N. Najm, "Verification and codesign of the package and die power delivery system using wavelets," *IEEE Trans. Computer-Aided Design*, vol. 29, no. 1, pp. 92–102, Jan. 2010.

[15] M. Avci and F. N. Najm, "Early P/G grid voltage integrity verification," in *Proc. Int. Conf. Computer-Aided Design (ICCAD)*, 2010, pp. 816–823.

[16] C.-K. Cheng, P. Du, A. B. Kahng, G. K. H. Pang, Y. Wang, and N. Wong, "More realistic power grid verification based on hierarchical current and power constraints," in *Proc. Int. Symp. Physical Design (ISPD)*, 2011, pp. 159–166.

[17] N. H. Abdul Ghani and F. N. Najm, "Fast vectorless power grid verification under an RLC model," *IEEE Trans. Computer-Aided Design*, vol. 30, no. 5, pp. 691–703, May 2011.

[18] P. M. Morgado, P. F. Flores, J. C. Monteiro, and L. M. Silveira, "Generating worst-case stimuli for accurate power grid analysis," in *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation*, 2009, pp. 247–257.

[19] P. M. Morgado, P. F. Flores, and L. M. Silveira, "Generating realistic stimuli for accurate power grid analysis," *ACM Trans. Design Automation of Electronic Systems*, vol. 14, no. 3, article 40, May 2009.

[20] P. Du, X. Hu, S.-H. Weng, A. Shayan, X. Chen, A. E. Engin, and C.-K. Cheng, "Worst-case noise prediction with non-zero current transition times for early power distribution system verification," in *Proc. Int. Symp. Quality Electronic Design (ISQED)*, 2010, pp. 624–631.

[21] N. Evmorfopoulos, M.-A. Rammou, G. Stamoulis, and J. Moondanos, "Characterization of the worst-case current waveform excitations in general RLC-model power grid analysis," in *Proc. Int. Conf. Computer-Aided Design (ICCAD)*, 2010, pp. 824–830.

[22] G. H. Golub and C. F. Van Loan, *Matrix Computations*, 3rd ed., The Johns Hopkins University Press, 1996.

[23] H. Qian and S. S. Sapatnekar, "Stochastic preconditioning for diagonally dominant matrices," *SIAM Journal on Scientific Computing*, vol. 30, no. 3, pp. 1178–1204, Mar. 2008.

[24] The MOSEK Optimization Software, http://www.mosek.com.