Chapter Title:

Analysis and Synthesis of Frequency-Diverse Ultrasonic Flaw Detection System using Order Statistics and Neural Network Processors

Abstract:

Ultrasonic imaging has been an essential tool for nondestructive evaluation of materials and flaw detection. However, flaw detection in the presence of microstructure scattering noise is a challenging problem. This chapter presents frequency-diverse ultrasonic detection algorithms which are essential to decorrelate the microstructure scattering noise and to enhance the visibility of echoes associated with defects in materials. In particular, the performance of ranked order statistics processors (such as minimum, median and maximum detectors) is examined using both theory and ultrasonic experimental measurements. Furthermore, this chapter gives emphasis to the concept of split-spectrum processing combined with neural networks as post processors to achieve improved flaw detection. Neural networks, because of trainability, offer an exceptionally robust performance and are capable of outperforming conventional detection techniques such as minimum, median, average, geometric mean, and polarity threshold detectors. An FPGA-based case study is presented for demonstrating the real-time operation of the ultrasonic flaw detection algorithms. Architecture details and implementation results with various Hardware/Software partitioning schemes are discussed.+

Keywords: Ultrasound, nondestructive evaluation, split-spectrum processing, neural networks, order statistics, flaw detection

Analysis and Synthesis of Frequency-Diverse Ultrasonic Flaw Detection System using Order Statistics and Neural Network Processors

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1.1 Introduction

In ultrasonic nondestructive evaluation (NDE) applications such as flaw detection, presence of high scattering noise poses a significant and challenging problem. This chapter presents techniques based on frequency-diverse ultrasonic imaging which induces significant statistical variation in scattering noise or speckles. In particular, the Split-Spectrum Processing (SSP) technique which performs subband decomposition and post-processing detection methods including Order Statistics (OS) and Neural Networks (NN) are discussed in detail. Adaptive learning capability of neural networks facilitates robust detection performance. Experimental results are presented for comparison of flaw-to-clutter visibility improvement with the proposed techniques. Finally, an FPGA based hardware platform is presented for System-on-Chip (SoC) realization of a real-time ultrasonic imaging system. This platform supports multiple embedded architectures including software-only, hardware/software co-design and hardware-only designs illustrating the possible trade-offs between hardware resources and system throughput. This chapter is concluded with a discussion of recent and future trends in real-time ultrasonic imaging.

1.2 Ultrasonic flaw detection techniques

In ultrasonic imaging, coherent noise resulting from the microstructure of materials consisting of a large number of complex and randomly distributed scatterers often mask the target echo to an extent that misdetection become the norm rather than an exception. Scattering noise known as clutter is a common

problem which affects a wide range of detection and imaging applications including radar, optics and sonar. When scatterers are stationary, as is the case in ultrasonic imaging, the clutter suppression cannot be achieved by signal averaging. Furthermore, clutter and target echoes span the same frequency range and signal filtering is also ineffective. Nevertheless, it is feasible to decorrelate clutter and improve target visibility by shifting the frequency band of the transmitter/receiver (using multi channels) and to obtain a set of frequency-diverse signals. The clutter decorrelation by frequency diversity (also known as frequency agility when frequency shifts from pulse to pulse using a single channel) for radar target detection dates back to sixties (Beasley and Ward, 1968; Lind, 1970; Barton, 1977). Hence, the averaging of the decorrelated received clutter signals results in signal-to-clutter ratio enhancement. In eighties and nineties, frequency-diverse detection for both ultrasonic imaging and radar target detection applications has been explored (Bilgutay et al., 1979; Newhouse et al., 1982; Saniie et al., 1990; Saniie et al., 1991; Saniie and Nagle, 1992). These investigations resulted in development of the theory and applications of signal subband decomposition followed by the Bayesian (Saniie et al., 1992) and Order Statistics (Saniie et al., 1990; Nagle and Saniie, 1995) post detection processors.

A typical ultrasonic pulse-echo measurement setup for flaw detection using a 5 MHz transducer is shown in Fig. 1.1, and experimental ultrasonic signal consisting of grain scattering and flaw echo obtained from a hole inside a steel block is shown in Fig. 1.2 (top trace). Fig. 1.2 (bottom trace) shows the improved flaw echo visibility using frequency-diverse order statistic (i.e., minimum) processor which will be discussed throughout this chapter.

1.2.1 Split-spectrum processing

In ultrasonic imaging of materials, an effective method of obtaining frequency-diverse information is through split-spectrum processing of the broadband echoes (Bilgutay et al., 1979; Newhouse et al., 1982). The SSP procedure has five steps as shown in Fig. 1.3. The first part is data acquisition. The second step,

Fast Fourier Transform (FFT) gives the frequency spectrum of the received echo signal. Third step, several filters split the spectrum into different frequency bands as shown in Fig. 1.4. Next step, inverse FFT gives the time domain signal of each individual frequency band. The signals from each individual frequency band are first normalized and then passed into a post processing block for detection. This detection processor can employ different techniques such as averaging, minimization, order statistic filters, or Bayesian classifiers (Saniie et al. 1988, Saniie et al., 1991; Saniie and Nagle, 1992; Saniie et al., 1992a; Saniie et al., 1992b).

SSP performance is greatly influenced by the number of bandpass filtering channels (or observations) across signal spectrum, the correlation between the observations, and statistical information in each channel. Increasing the number of channels increases the likelihood of separating flaw and grain echo information. However, there exists only a limited number of information bearing frequency bands. This means that increasing the number of channels would result in many observations that only contribute to grain (clutter) echo information. Another trade-off is between the bandwidth of the channels and the degree of overlap ~~amount~~ between channels. If the channel bandwidth is too small, flaw echo information is concealed due to resolution loss. Excessive overlap between channels on the other hand, results in disproportionate correlation among the channels. Correlation is not as critical for ultrasonic flaw detection performance as choosing the proper frequency range containing significant flaw echo information.

In order to enhance the visibility of flaw echo masked by clutter, SSP method utilizes a post-processor for combining all the incoming information from subbands. This post-processor reconstructs the time-domain signal with the objective of obtaining maximum flaw-to-clutter ratio (FCR). Several types of processors can be used to extract the flaw echo information. Minimization, in particular, is very effective in suppressing the clutter echoes when flaw echo information exists in all the observation channels (Saniie et al. 1991). If too many null-observation channels (frequency bands where no flaw echo information

appear due to the frequency-dependent attenuation) be present, then the minimization processor may not achieve the desired FCR improvement. Fig. 1.5 shows channels that do not contain flaw echo information. Under these circumstances, other post-processing methods such as median or maximization may offer more robust detection performance. Similar to minimization, median and maximization methods are called order statistics filters which will be discussed in more detail in Section 1.5. Order statistics have been developed in the statistics field and successfully employed in ultrasonic target detection (David, 1981; Saniie et al., 1991; Saniie and Nagle, 1992).

In the following section, the frequency analysis of the ultrasonic signals is presented and the frequency diversity between clutter (i.e., grain scattering echoes) and the flaw echoes is highlighted. This difference in frequency response can be exploited for robust flaw detection algorithms.

1.2.2 Frequency analysis of ultrasonic signals

In the Rayleigh scattering region, grain (i.e., microstructure) scattering results in an upward shift in the expected frequency of the broadband ultrasonic signal. This is not the case for flaw echoes since flaws are generally larger in size than the grains and behave like geometrical reflectors. In fact, flaw echoes often display a downward shift in their expected frequency caused by the overall effect of attenuation. This downward frequency shift of the flaw is a productive attribute since the grain noise and flaw echoes are concurrently received and preprocessing methods can improve the flaw-to-clutter ratio. If the information-bearing frequency bands that are dependent on the specific characteristics of materials are known *a priori,* optimal bandpass filtering can be employed (Saniie and Nagel, 1992).

The exploration of the frequency content of ultrasonic backscattered signals can give spectral energy profiles corresponding to the grains and the larger geometric reflectors (i.e., defects). The energy loss and attenuation of ultrasonic signals are caused by the microstructure of the propagating media through which

scattering and absorption occurs. The intensity of scattering is a non-explicit function of the average grain diameter, ultrasonic wavelength, inherent anisotropic character of the individual grains, and the random orientation of the crystallites. In the Rayleigh region (i.e., the wavelength is larger than the size of the grains), the scattering coefficient varies with the average volume of the grain and the fourth power of the wave frequency, while the absorption coefficient increases linearly with frequency (Papadakis, 1965; Saniie et al., 1988). Therefore, the attenuation coefficient can be modeled as:

$$\alpha(f) = a_1 f + a_2 \overline{D}^3 f^4 \qquad [1.1]$$

where a_1 is the absorption constant, a_2 is the scattering constant, $\overline{D}$ is the expected value of the grain diameter, and f is the transmitted frequency.

The composite effects of scattering and attenuation due to grains can be characterized in terms of transfer functions derived from the spectrums of measured signals obtained in the ultrasonic pulse/echo measurement mode as shown in Fig 1.1. The front surface echo, $r_f(t)$, represents the combined effect of the far-field transfer function of the transducer impulse response $U(f)$, the ultrasonic pulser, receiver amplifier, and the water propagation path. In the RF frequencies (1-15MHz range), the characteristics of the pulser /receiver and water propagation path are frequency independent. Therefore, the transfer function of the received front surface echo signal is proportional to the transfer function of the transducer impulse response (Saniie and Nagel, 1992):

$$R_f(f) \propto U(f) \qquad [1.2]$$

The spectrum of the received backscattered signal form the back wall of the specimen (see Fig. 1.1), $R_b(f)$, can be modeled as

$$R_b(f) \propto A(f)U(f) \qquad [1.3]$$

where $A(f)$ is the transfer function corresponding to the attenuation characteristics of the signal propagation path within the specimen. In Fig. 1.6(a), a heuristic evaluation of $A(f)$ is given by the ratio

of the spectrums of the above measured signals $\frac{|R_b(f)|}{|R_f(f)|}$ using a steel block with an average grain size of 50 microns and a 5 MHz ultrasonic transducer. This figure clearly exhibits that there is a definite shift or emphasis of the lower frequencies. This indicates that echoes associated with flaws significantly greater in size than the echo wavelength, have dominant energy in lower frequencies.

The microstructure scattering transfer function, *S(f)*, can be obtained by the ratios of the expected spectrum of the grain echoes, $r_g(t)$ and the spectrum of back surface echo $r_b(t)$, $|R_g(f)|/|R_b(f)|$, which is displayed in Fig. 1.6(b). These results indicate that grain scattering causes the lower frequencies to become poorly backscattered (i.e., attenuated) resulting in an upward shift in the expected frequency of the grain spectrum. Thus, in order to take advantage of this property in flaw detection, frequencies where the grain scattering is minimal should be emphasized in order to maximize the flaw-to-clutter ratio (Saniie and Nagel, 1992).

In summary, both flaw and grain echoes display predictable frequency dynamics associated with the physical properties of the materials. Experimental results (see Fig. 1.6) also indicate the frequencies where high flaw-to-clutter ratios exist and this information can be utilized in the preprocessing stage of the block diagram of Fig. 1.3. These characteristics are advantageous and lead to obtaining an optimal frequency range containing high flaw-to-clutter ratios for the SSP of the preprocessing stage. In the next section, order statistics method is discussed in detail which can utilize the frequency diversity of ultrasonic signals for improved flaw detection.

1.2.3 Order Statistics (OS) processors

As shown in the preceding section, the disparity in the energy of lower frequencies of the grains and flaws allows bandpass filtering techniques to extract the flaw information in the preprocessing stage of Fig. 1.3.

However, additional improvements in flaw-to-clutter ratio and resolution can be obtained through SSP techniques that focus on the statistical information in the frequency region of high flaw-to-clutter ratios.

In SSP, after subband decomposition, the next step is to use the partially uncorrelated observations and make use of statistical differences in the channels (i.e., corresponding to random phase information in the received grain echoes) to improve the flaw-to-clutter ratio and resolution of the flaw echoes. The order statistics filter is shown to be a quantile estimator (Saniie et al., 1990) of the input density function that describes a specific point on the probability distribution function. The performance of the detector can be improved by choosing the position of the estimate where there are large statistical differences between the two hypotheses (flaw present, H_1 , or not present, H_0).

The order statistics (David, 1981) filter ranks a set of *n* input values corresponding to simultaneously sampled values of the *n* channels of the SSP output, (x_1,x_2,x_3,…x_n),

$$x_{(1)} \leq x_{(2)} \leq x_{(3)} \ldots \leq x_{(n)} \qquad [1.4]$$

where a given order or rank, *r*, is chosen and $x_{(r)}$ is passed to the output. This processor is the median filter when $r = (n + 1)/2$ (for odd *n)*, the maximum filter when $r = n$ and the minimum filter when $r = 1$.

An important step for optimizing the OS filter involves finding the relationship between the input and output statistical behavior of the data. Assuming the input observations, *x*, are independent and identically distributed with distribution $F_X(x)$, the order statistic is known to be a consistent and asymptotically unbiased estimator of the quantile (Saniie et al., 1990):

$$\lim_{\substack{n\to\infty \\ r\to\infty}} E\left[X_{(r)}\right] = F_X^{-1}(u_r) \qquad [1.5]$$

where $u_r = (r-1)/(n-1)$ is a constant (i.e., normalized rank) bounded between zero and one, and $E\left[X_{(r)}\right]$ is the expected value for the output of OS filter. In the aforementioned limit, both *r* and *n* approach infinity but u_r remains a finite ratio of *r* and *n*. For infinite *n*, the OS filter is an unbiased

quantile estimator. With finite observations, *n*, the estimate will have some dispersion about the quantile value, u_r, that allows the values of neighboring quantiles to influence the output. It should be noted that the performance of the OS filter will generally improve with increasing observations *n* since the variance will decrease (i.e., the effect of random nature of the grains echoes will be reduced). The lower-ranked order statistics have been shown in the past to give improvement in the resolution of echoes and the flaw-to-clutter ratio (Bilgutay and Saniie, 1984) provided all channels contain significant flaw information.

It can be seen that the parameters *r* and *n* can be used so that the OS filter emphasizes particular regions in the distributions of the input signals. The OS filtering operation censors the signal values outside this quantile region from the decision rule. This property is useful when the classes of signals exhibit a distinctive statistical difference over a limited range of quantiles, such as what may occur with speculary reflective targets.

The optimal rank is dependent on the input distributions that are illustrated by the following two examples (Saniie et al., 1991). In the first example, we assume the number of observations is 25, and the target-plus-clutter observations (i.e., flaw echoes) are *Chi* distributed with skewness equal to 0.566 in *Weibull* clutter (i.e., grain echoes) with a skewness equal to 1.05. Their respective inverse distribution functions are shown in Fig. 1.7. The performance of the OS filter can be seen in Fig. 1.8 where the probability of detection for all possible rank values ($r = 1, 2, 3, \ldots, 25$) is plotted for 0dB and 2dB signal-to-clutter ratios (SCR). The lower ranks perform significantly better since there is greater separation in smaller quantile regions where $u < 0.6$, as shown in Fig. 1.7. Here, *u* represents the normalized rank with respect to the total number of observation channels and it is always less than or equal to 1. Note that the optimal rank occurs at $r = 2$ for the lower SCR and $r = 4$ for the higher SCR. For the higher SCR, the optimal choice is less critical, since for any *r* value from 1 to 10, the OS filter shows good performance. In the second example, both target-plus-clutter and clutter are Rayleigh distributed with skewness equal to 0.63 where the inverse distributions are as shown in Fig. 1.9. In Fig. 1.10**,** the optimal *r* is 19 for the

lower SCR (3db) and 20 for the higher SCR (6dB). For the high SCR, the robustness of the upper ranks is self-evident from the visual examination of the inverse distributions of Fig. 1.9, and will increase as the input SCR increases.

In the next section, we present an alternative post-processing technique based on neural networks which offers superior and more robust flaw detection performance.

1.3 Neural network detection processor

Neural networks are nonlinear mapping processes that allow training and adaptability for signal classification applications (for example, Cichocki and Unbehauen 1993; Gurney 1997; Haykin, 2008). The learning process enables neural networks to recognize the target patterns without mathematical models of the target signals which often are unknown. There are several key advantages of neural networks:

- Neural networks are trained by desired result. This means that no mathematical model is necessary.
- Neural networks approximate unknown systems which include non-linear models. This non-linearity is an important property which enhances the network's classification or approximation capabilities without estimating any statistical parameter.
- Neural networks have parallel structure which provides fast performance for real-time detection applications.

In this study, a three-layer feedforward neural network (Hornik 1989) is used as the post-processor of the ultrasonic flaw detector. Neural networks provide superior flaw-to-clutter ratio performance when compared to other post-detection processors. Furthermore, hardware realization of neural networks for real-time ultrasonic target detection systems is feasible (Yoon et al., 2006).

1.3.1 Neural networks architecture

A neural network contains many nodes which are connected to each other. Each node consists of a basic computation function and an activation function. Computation unit processes the input signals and sends them to the activation function. The activation function unit produces the output of the node which can be the final output of a neural network or the input of another neural node. The neural networks can be classified to be i) feedforward neural networks, or ii) recurrent neural networks. The former has feedforward structure where neural nodes receive the input data and pass the data to next adjacent neural nodes without any feedback. In this study, a three layer feedforward neural network is designed as a post processor of the ultrasonic target detection system.

An objective function is used to train the neural networks. The squared error function which is computed between the output of neural networks and the desired output is used as the objective function. The objective function measures how differently neural networks behave from the desired outputs. The goal of the neural network learning is to find the weight coefficients where the objective function reaches the minimum value. In this research, the backpropagation algorithm is used for training the neural network.

1.3.2 Neural network model for SSP post processing

A three-layer feed-forward neural network with SSP is shown in Fig. 1.11. The nodes in the first layer send SSP data to the second layer. The neural nodes in the second layer which are called hidden layer nodes receive the weighted inputs from the first layer and then perform a nonlinear mapping calculation using the activation function. The output neural nodes in the third layer sum up the weighted inputs from second layer. The model of neural nodes is shown in Fig. 1.12. The weight coefficients w_{ji} indicates the i_{th} input and j_{th} node.

The general neural node model can be expressed by

$$y_j = \varphi(\sum_i w_{ji} x_i + b_j) \quad [1.6]$$

where x_i is a set of inputs of each neuron, y_j is a set of outputs of each neuron, and b_j is a set of bias of each neuron. Each input is multiplied by a weight coefficient w_{ji}. The subscript *ji* refers to the input *i* in neuron *j*. The term φ is an activation function.

There are several properties for the activation function. First, the activation function of hidden layer in three layer neural network needs to be nonlinear. Second property is the saturation which ensures the weights and activations are bounded. The third property is continuity and smoothness. The backpropagation algorithm needs the derivative of the activation function during its learning process. In this research, the activation function used in the hidden layer is the sigmoid function which can be expressed by

$$\varphi(x) = (1 + e^{-x})^{-1} \quad [1.7]$$

1.3.3 Backpropagation learning process

The learning process allows neural networks to adapt to the environments of particular applications. The learning step takes place through iterative process of adjusting weight values. We adapt the backpropagation algorithm (Masters, 1993) to train the neural networks for ultrasonic target detection system. In the learning process, it is important to select the initial weights randomly since the training result can be limited to a local minimum based on the initial values. After the training, the weight coefficients are fixed and then used for the other input sets. Additional training for neural networks is only necessary when the environments of the application are changed.

The activation function of hidden nodes has an important role in the nonlinear mapping process. The output of the sigmoid function reaches one or zero when the input approaches a positive or negative infinity value. This means that the output will be a one or zero value when the input is very large. This may cause the nonlinear mapping process of neural networks to fail. To avoid undesirable condition, the input data is normalized between -1 and 1.

To train the neural networks for the ultrasonic flaw detection, we used an experimental ultrasonic data which has a flaw in a priori-known location. The desired output data is made of all *zero* values and a *one* value at the known flaw location. The initial values of weights and bias are randomly selected. The number of input nodes is the same as the number of SSP channels and only one output node is used. It is important to note that the number of hidden nodes affects the performance of the neural networks. In this research, we chose 5 hidden nodes for neural networks after several trials. An objective function such as the sum of the squared error function is necessary to reach the minimization criterion to complete the learning process. If the minimization criterion of the objective function is not met, we increase the number of epoch which corresponds to a single presentation of all patterns in the training set. If the criterion is still not met with the large number of epochs, increasing the number of hidden nodes can fix the problem. However, increasing the number of epoch or hidden nodes takes longer learning time.

1.3.4 Software implementation of the neural networks

The neural network based SSP post-processor is implemented in MATLAB software for performance evaluation. The experimental data are used for both training and detection test. Fig. 1.13 shows the data for training and the desired output data. The backpropagation learning algorithm computes the mean-squared error of the difference between the desired output and real output value and adjusts the weight and bias coefficients until the mean-squared error function reaches a predetermined minimum value. After training, the neural network is expected to respond to flaw echoes if the input has flaw signals. The neural

networks provide the big pulse as a flaw echo and the small value for the clutter echoes since one was assigned to a flaw and zero was assigned to clutter echoes during the learning process. In the design of the neural networks, 8 channel SSP and 5 hidden nodes have been used. The result of trained neural networks flaw detector is shown in Fig. 1.14. For major changes that occur in the experimentation setup (such as different transducer types, different frequency of interrogation or change in material types), it may be necessary to re-train neural network weight coefficients.

1.4 Flaw detection performance evaluation

In this section, neural networks are compared against other conventional post-processing flaw detection methods such as order statistics (minimum, median, averaging), geometric mean (Xin, 1991) and polarity detectors (Bilgutay et al., 1989). The mathematical expressions of these techniques are given as the following:

Average detector:

$$\phi_{av}(n) = \frac{1}{k}\sum_{j=1}^{k}\left|z_j(n)\right| \qquad [1.8]$$

Median detector:

$$\phi_{med}(n) = \text{median}[\left|z_j(n)\right|,\ j = 1,2,...,k] \qquad [1.9]$$

Minimum detector:

$$\phi_{\min}(n) = \min[\left|z_j(n)\right|,\ j = 1,2,...,k] \qquad [1.10]$$

Geometric mean detector:

$$\phi_{gm}(n) = \sqrt[k]{\prod_{j=1}^{k}\left|z_j(n)\right|} \qquad [1.11]$$

Polarity detector:

$$\phi_p(n) = \begin{cases} & \text{if } z_j(n) > 0 \text{ or } z_j(n) < 0 \\ z(n) & \text{for all } j = 1, 2, \ldots, k \\ & \\ 0 & \text{otherwise} \end{cases} \qquad [1.12]$$

where $z(n)$ is the measured broadband signal, $z_j(n)$ is the SSP output of channel j, and k is the total number of the SSP channels.

The neural networks and other detection methods are implemented and compared with experimental ultrasonic data. For performance analysis and testing, the experimental A-Scan data from a steel block (type 1018, grain size 50μm) are acquired and analyzed. A Panametric (type 5052) pulser/receiver is used to drive the ultrasonic transducers and to receive the ultrasonic backscattered echoes. The received echo signals are then converted to digital data for split-spectrum processing. The A-scan measurements were conducted using a broadband unfocused ultrasonic transducer of 0.5inch diameter with 5MHz center frequency. Data were acquired with 100MHz sampling rate and each sample is 8 bits. 1024 data points for each A-scan represents approximately a depth of 2.5 cm. The steel block has several holes (1.5 mm diameter) at known, separate locations. All the A-scan measurements probe the hole positions within the steel block. For performance analysis, flaw-to-clutter ratio (FCR) is evaluated by finding the maximum flaw echo amplitude after the post-processing step. This value is compared with the largest amplitude of clutter echoes. Therefore, *FCR* can be defined as

$$FCR = 20 * log10(F/C) \qquad [1.13]$$

where F is the maximum flaw echo amplitude and C is the maximum clutter echo amplitude.

Fig. 1.15 shows experimental data in the time domain (Fig. 1.15(a)) and frequency domain (Fig. 1.15(b)) as well as the frequency spectrum of the 8-channel SSP bandpass filters (Fig. 1.15(c) and Fig. 1.15(d)).

Fig. 1.15(c) covers the frequency range where the flaw echo exists in all subbands (no null observations). Fig.1.15(d) shows the frequency spectrum of the 8 subband filters which cover the full frequency spectrum of the original measured signal. In this case, some subband filter outputs (higher frequency bands) may have very low *FCR* and are considered to be null observations. Therefore, a robust flaw detection method which offers minimal sensitivity to the frequency coverage of filters is desirable (Yoon et al., 2007). The comparison results of various detectors applied to SSP channels covering the low frequency region (ranging from 1.5MHz to 6 MHz) are shown in Fig. 1.16. In this frequency region, there are no null observations. With the neural network (NN) detector, the flaw echo is sharply detected without visible clutter. The other detectors also detect the flaw. Table 1.1 also confirms that the neural network outperform the other techniques. The average FCR of neural network detector is 46.8dB; however, the average FCR of minimum detector is 7.9dB when only low frequency region is covered. The FCRs of the other detectors are significantly lower than minimum detector.

Fig. 1.17 shows the comparison results of various detectors applied to SSP channels covering the full frequency spectrum (ranging from 1.5 MHz to 9 MHz) of the ultrasonic data. It is important to point out that null observations exist in this frequency range. Neural networks can still detect the flaw signal; whereas the other detectors barely detect or fail to differentiate the presence of the flaw echo. In Figures 1.16 and 1.17, NN output values are close to 0 for clutter echoes and close to 1 for target echoes. For other detectors, output values are normalized to -1 and 1, or 0 and 1 for presentation purposes. Table 1.1 shows the *FCR* results of the original input data and six different post-processors with two different subband filters coverage. These results confirm that the NN detector not only outperforms the conventional flaw detection methods but also shows less vulnerability to null observations (third row in Table 1.1).

In the next section, we present an FPGA based hardware platform for real-time ultrasonic flaw detection applications. Architecture details and implementation results are discussed.

1.5 System-on-chip implementation – a case study

A test system was designed and built to process real-time ultrasonic data utilizing the SSP algorithm. An overview of the test system is shown in Fig. 1.18 (Weber et al., 2011). The system is composed of three major components. The first is a host computer, providing control of the system to the user and presentation of all data and results. Running on the host computer is the application software developed to enable communication with the hardware components implemented in an XtremeDSP unit produced by Nallatech (Nallatech 2005). This XtremeDSP unit combines a Xilinx Virtex 4 FPGA with dedicated ADC and DAC chips into a convenient package. The final component is the transducer and pulse generator. The pulse generator takes in a low voltage TTL level signal and generates the high voltage pulse to excite the transducer. In addition, it provides the acquisition of the reflected echo signal.

1.5.1 Hardware realization

Tasks necessary for real-time ultrasonic detection system are broken into three modules, communications, signal processing, and signal capture. All three modules are packaged in a Xilinx Virtex 4 FPGA (Xilinx, 2008). This FPGA is provided on the Nallatech ExtremeDSP development kit as the main user FPGA. This board also provides other components used in the system. They include dedicated ADC and DAC chips, fixed and programmable oscillators, a dedicated Virtex-II FPGA for clock management, and a dedicated Spartan-II FPGA for PCI/USB communications control.

The *signal capture* module controls the firing of the transducer and capturing of all echo data coming in from the dedicated ADC chips. It also provides a level of pre-processing, by adding a configurable amplifier to the incoming data. It is important to note that the clock domain in this module is separate from the data processing element. The result of this is that the sampling rate of the device is independent

of the clock rate of the processing unit. This enables optimization of the clock rate and sample rate independently for maximum performance.

The *communication module* provides an interface to the host PC and oversees all communications. It provides two primary services. The creation of a register file and the ability to access those registers through a memory mapped interface and a DMA interface that can be easily connected to internal Block RAMs (BRAMs). It accomplishes this through the aid of a separate dedicated FPGA component. This FPGA provides all the PCI or USB interfacing requirements, simplifying the design to be more manageable. The system also provides 16 separate channels for DMA access. These 16 channels can be connected to any internal BRAM within the FPGA. This is very beneficial in debugging and verification of the system.

The *signal processing module* implements the SSP algorithm. It performs all the transformations and computations to produce the final output data. It gathers its input data from the signal capture module, and obtains parameter values from the communication module. As data flow into the module, it is first transformed to the frequency domain through an FFT module. The FFT module used is a Radix-2 based IP core provided by Xilinx (Xilinx, 2010). This module is highly optimized by Xilinx to take full advantage of the dedicated DSP blocks within the Virtex 4 device. As a design configuration parameter, FFT operation is implemented with an 8-bit input precision. The data is allowed to dynamically grow to a 19-bit output, which is then truncated to 16-bits to be passed on to the rest of the design. The output of the FFT module is then decomposed by bandpass filters. The filters are dynamic in their set points. Both the center frequency and bandwidth of the filters is controlled by user writable registers in the communication module. This allows the user to change the bandpass filter parameters without reconfiguration of the FPGA device. These filter parameters are chosen to optimize the subbands. They are selected to cover the entire bandwidth of the echo response.

The subband channels are then transformed through the use of inverse FFT (IFFT) modules. Since all subbands are independent, parallel IFFT modules are used to increase performance. The IFFT modules, like the FFT module, are highly optimized Xilinx IP cores. They take the 16-bit input and allow it to grow to 27-bits. The resulting data are then processed without further truncation. By eliminating truncation, a very high dynamic range is achieved. This helps the hardware design to perform very closely to the ideal software representation.

1.5.2 Application software

In order to maintain the modularity and reusability, a software package has been designed in a layered manner (see Fig. 1.19). At the most basic level is the PCI/USB communication drivers, controlled by the PC operating system. On top of that is the communication application programming interface (API) developed by Nallatech. This provides support for basic communications of two types between the host PC and the hardware components. It provides memory map register access and 16 DMA channel access to the internal memory blocks. Furthermore, in order to enable a simple interface to the hardware, a new MATLAB toolbox has been developed. This toolbox acts as a wrapper around Nallatech developed API providing a more convenient design for the most common communications between the host PC and the hardware.

In the following sections, a full hardware implementation is compared with various Hardware/Software (HW/SW) partitioning schemes.

1.5.3 Hardware/software co-design

A hardware/software co-design approach (Micheli and Gupta, 1997) enables a more robust design which can comfortably meet the system requirements. The hardware/software design has been developed with

the Xilinx Embedded Development Kit (EDK) and targeted at an FPGA device with an embedded softcore Microblaze processor.

Initially all processing is done in software through Microblaze processor. In order to improve performance of the design, the full execution of the FFT transform is realized in the hardware domain through the addition of an FFT accelerator co-processor. The FFT accelerator co-processor is implemented as a custom VHDL based design. This accelerator is interfaced to the Microblaze processor through the On-Chip Peripheral Bus (OPB) as shown in Fig. 1.20. By keeping the accelerator, processor, and bus structure all within the same FPGA device, it allows for very high performance. A software driver is created and the software design is updated to pass data to the accelerator and receive back the FFT results. This accelerator demonstrates the integration of hardware design techniques with software design.

1.5.4 Software and Hardware Performance Evaluation for SSP

The SSP detection performance of the software architectures (C code running on an embedded Microblaze processor) perform identically to the theoretical Matlab implementation. This performance result is expected. The software implementations use a floating point representation of the data, the same as the internal representation within Matlab. Therefore, there is no change in performance for the software implementations.

On the other hand, both the hardware architectures and the hardware/software co-design with the FFT accelerator use fixed point hardware based FFT processing units. Due to the fixed point representation, and limited wordlength, there is some inherent data imprecision when calculating the FFT transforms. The final impact of this result is a decrease in overall system performance. For ten different data sets, the performance for the hardware architectures can be seen in Table 1.2.

It is also important to notice that the 8 channel implementation is able to achieve results much closer to the theoretical ideal. In addition to the overall performance, the 8-channel implementation exhibits a standard deviation of 1.98 compared to a standard deviation of 3.48 for the 4-channel approach. Hence, the 8 channel implementation provides a much more robust performance. The reason for this more robust performance is due to the placement of the window filters. The 8 channel result is able to use smaller filters with a similar overlap, and still be able to cover a larger portion of the frequency spectrum.

1.5.5 Execution time

For ultrasonic imaging, real-time rate is considered to be a processing rate exceeding 1 kHz. This gives only a short 1 ms time window to perform all capture and processing of data. The execution time result for all the architectures is shown in Table 1.3. This table goes into further depth by breaking down the execution time for each algorithmic processing step.

It can be shown that the pure software approaches fail to reach the real-time requirement. The basic software implementation with only a simple processor without a floating-point unit (FPU) struggles to perform all the computations. With the move to a more complicated microprocessor, incorporating a FPU unit, the design is able to improve to a time of 37.7ms, although still well below the required rate. Both of these designs demonstrate that a software only solution is not reasonable for this application.

Table 1.3 also shows the execution time for both radix-2 and radix-4 pure hardware architectures. These implementations aim for high performance using fast hardware processing elements and a highly parallel implementation, with multiple FFT cores for faster processing. Correspondingly, the designs easily exceed the processing rates required and provide orders of magnitude improvement in execution time compared to the software implementations, being 370 times faster.

As expected the hardware/software co-design architecture is able to achieve a middle ground performance between the two pure designs. The hardware/software co-design is able to achieve a performance rate of 3.05ms. While the design currently does not meet the real-time requirements, it is close enough to be optimized to achieve the needed performance. Through the use of final optimization of clock rate and code optimization it would be reasonable to expect performance gains to meet the requirements.

1.5.6 Resource usage

Resource usage is characterized with the three major resources provided within the Xilinx Virtex 4 FPGA device; logic slices, block RAMs, and DSP48s. Logical slices provide the fundamental configurable logical resources in an FPGA device. They provide the ability to perform all logic, arithmetic, and ROM storage and have addition elements to enable distributed RAM storage. The particular device used provides support for up to 30,720 slices. For larger RAM storage needs, the device also provides 192 distributed dual port 18 Kbit RAM blocks. The final important resource items provided are 192 DSP48 elements (Xilinx, 2007).

The evaluation of these three resources is a good representation of the cost of the implementation. The resource consumption for all the designs is shown in Table 1.4. The resource usage tends to follow the trend in execution time performance. As the designs become more complex, they are able to achieve higher performance rates.

1.6 Future trends

A common challenge today for ultrasonic imaging is the synergetic integration of sensor devices, signal processing units and miniaturization. There has been an increasing demand for portable, handheld sensor

devices which can operate not only in controlled environments such as laboratories or clinics but also in the field. These devices could have a major impact on the ease of use and simplification of the diagnosis processes for medical practitioners or test engineers. However, there are major design challenges for the development of compact sensor devices. These challenges are:

Low power consumption: Portable and handheld devices use battery power. Consequently, power consumption of the devices should be kept to a minimum in order to obtain a truly field operable device.

Compact size: Besides power consumption, portable devices enforce a very limited design space for the hardware components. An ideal solution would be tighter integration of the components with system-on-chip (SoC) design. SoC provides a single chip solution for complete system implementation, with built-in embedded input/output interfaces, control units-processors, and data processing elements.

High computational rate: Real-time operation with instantaneous results is a critical requirement for ultrasonic systems. Therefore, the hardware and software components should be designed primarily to cope with very complex computational requirements of real–time systems.

Adaptability: The evolving standards and/or introduction of new testing, imaging or diagnostic techniques can cause a sensor device to become out-dated in a very short life-span. An ideal system should be designed in such a manner that the hardware kernel can be updated in order to make it future proof. It is also important to have a feature-proof system in which more functionality can be added.

Network Connectivity: The sensor device should be capable of transmitting and receiving over the internet for remote data access.

Integration with MEMS sensors: A complete system-on-chip solution necessitates using MEMS sensor arrays for imaging, target detection, and classification.

In order to meet all the design criteria, optimizations are required at both architectural level and algorithmic level. The following technology and signal processing trends are promising for next generation of ultrasonic imaging devices:

1. Development of time-frequency (T/F) algorithms for robust target (flaw) detection and estimation. The backscattered signal information in ultrasonic non-destructive testing is non-stationary due to frequency dependent scattering, attenuation and dispersion. The standard spectral analysis cannot determine the time of arrival of different frequency components in the signal. Joint T/F representations of such signals are more revealing. Therefore, T/F distributions such as Gabor Transform (GT), Wigner-Ville Distribution (WVD), Choi-Williams (CW) distribution and Wavelet Transform (WT) should be analysed for optimal ultrasonic flaw detection (Oruklu et al., 2009b).
2. Design and synthesis of adaptive system-on-chip architectures which can support dynamic reconfiguration of on-chip processing engines through internal switches and/or partial programming of FPGA devices.

Recently, similar multi-core and multiple Processing Element (PE) designs have been proposed in International Technology Roadmap for Semiconductors (ITRS) executive reports and conference proceedings: "*A possible ultimate evolution of on-chip architectures is asynchronous heterogeneous multi-core with hierarchical processors organization*" (Hutchby, 2007). Reconfigurable ultrasonic imaging architectures that conform to the "*More than Moore*" domain definitions of the ITRS should be designed for sustaining high computational capability and adaptability (Oruklu and Saniie, 2009a).

3. Sensor development and integration for System-in-a-Package (SiP) devices.

ITRS long-term projections also indicate the necessity of *System in a Package* (SiP) devices (ITRS, 2009). *System in a Package (SiP)* devices focus on full integration with sensors and actuators, based on a wide range of new technologies such as MEMS sensors. Correspondingly, MEMS actuators can be integrated with digital signal processing engines for a single chip solution in ultrasound imaging applications.

1.7 Further information

More information in this topic can be found in the journal publications; IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, Journal of the Acoustical Society of America, Ultrasonics (Elsevier) and in the proceedings of IEEE Ultrasonics Symposium, International Congress on Ultrasonics, and Acoustical Society of America meetings.

1.8 Conclusion

This chapter presented the theory and application of split-spectrum processing in ultrasonic flaw detection problems. Frequency diversity of grain and flaw echoes suggests that order statistics and neural network post processors can be used for flaw echo visibility enhancement. When statistical information in the observations deteriorates (e.g., null observations) and a priori information is not available, neural network post processors perform more robustly. Furthermore, a case study demonstrates that reconfigurable embedded systems are capable of real-time realization of ultrasonic imaging applications.

1.9 References

Barton D K (1977), *Frequency Agility and Diversity (Radars, Volume 6)*, Artech.

Beasley E and Ward E (1968), 'A quantitative analysis of the sea clutter decorrelation system with frequency agility', *IEEE Transactions on Aerospace and Electronic Systems*, 4, 468-473.

Bilgutay N M, Saniie J, Newhouse V, and Furgason E S (1979), 'Flaw-to-grain echo enhancement', *Proceedings of Ultrasound International Conference*, 152–157.

Bilgutay N M and Saniie J (1984), 'The effect of grain size on flaw visibility enhancement using split-spectrum processing', *Materials Evaluation,* 42, 808-814.

Bilgutay N M, Bencharit U and Saniie J (1989), 'Enhanced ultrasonic imaging with split-spectrum processing and polarity thresholding', *IEEE Transactions on Acoustics, Speech, and Signal Processing*, 1722–1732.

Cichocki A and Unbehauen R (1993), *Neural Networks for Optimization and Signal Processing*, Wiley

David H A (1981), *Order Statistics 2nd edition*, Wiley-Interscience.

Gurney K (1997), *An Introduction to Neural Networks,* CRC Press.

Gustafson B and As B (1964), 'System properties of jumping-frequency radars', Philips Telecommunications Review, 25, 70-76.

Haykin S (2008), *Neural Networks and Learning Machines (3rd Edition)*, Pearson.

Hornik K (1989), 'Multilayer Feedforward Networks as Universal Approximators', *Neural Networks,* v.2, pp. 359-366.

Hutchby J (2007), Emerging research devices, Japan, ITRS Conference. Available from: http://www.itrs.net/Links/2007Winter/2007_Winter_Presentations/06_ERD_2007_JP.pdf [Accessed January 18, 2011].

ITRS (2009), Executive summary, International Technology Roadmap for Semiconductors (ITRS), Available from: http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_ExecSum.pdf [Accessed January 18, 2011].

Lind G (1970) 'Measurement of sea clutter correlation with frequency radar', *Philips Telecommunications Review*.

Masters T (1993), *Practical Neural Network Recipes in C++*, Academic Press Inc.

Micheli G D and Gupta R K (1997), 'Hardware/software co-design', *Proceedings of IEEE*, 85, 349–365.

Nagle D and Saniie J (1995), 'Performance analysis of linearly combined order statistic CFAR detectors', *IEEE Transactions on Aerospace and Electronic Systems*, 31, 522-532.

Nallatech (2005), Virtex-4 XtremeDSP, Development Kit User Guide, Lanarkshire, U.K. Available from: http://www.xilinx.com/support/documentation/boards_and_kits/ug_xtremedsp_devkitIV.pdf [Accessed January 18, 2011].

Newhouse V, Bilgutay N, Saniie J and Furgason E (1982), 'Flaw-to-grain echo enhancement by split-spectrum processing', *Ultrasonics*, 59-68.

Oruklu E and Saniie J (2009), 'Dynamically reconfigurable architecture design for ultrasonic imaging', *IEEE Transactions on Instrumentation and Measurement*, 58, 2856-2866.

Oruklu E, Aslan S and Saniie J (2009), 'Applications of time-frequency distributions for ultrasonic flaw detection', *IEEE Ultrasonics Symposium*, 2000-2003.

Papadakis E P (1965), 'Ultrasonic attenuation caused by scattering in polycrystalline metals', *Journal of the Acoustical Society of America*, 37, 703-710.

Saniie J, Wang T, and Bilgutay N M (1988), 'Statistical evaluation of backscattered ultrasonic grain signals', *Journal of the Acoustical Society of America*, 84, 400-408.

Saniie J, Donohue K and Bilgutay N M (1990), 'Order statistic filters as postdetection processors', *IEEE Transactions on Acoustics, Speech, and Signal Processing*, 38, 1722-1732.

Saniie J, Nagle D and Donohue K (1991), 'Analysis of order statistic filters applied to ultrasonic flaw detection using split spectrum processing', *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, 38, 133-140.

Saniie J and Nagle D (1992), 'Analysis of order statistic CFAR threshold estimators for improved ultrasonic flaw detection', *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, 39, 618-630.

Saniie J, Wang T and Jin X (1992), 'Performance evaluation of frequency diverse Bayesian ultrasonic detection', *Journal of Acoustical Society of America*, 91, 2034-2041.

Weber J, Oruklu E and Saniie J (2011), 'FPGA-based configurable frequency-diverse ultrasonic target detection system', *IEEE Transactions on Industrial Electronics*, 58, 871-879.

Xilinx (2007), ExtremeDSP for Virtex-4 FPGAs user guide, San Jose,CA, Xilinx, Inc. Available from: http://www.xilinx.com/support/documentation/user_guides/ug073.pdf [Accessed January 18, 2011].

Xilinx (2008), Virtex-4 User Guide, San Jose, CA,Xilinx, Inc. Available from: http://www.xilinx.com/support/documentation/user_guides/ug070.pdf [Accessed January 18, 2011].

Xilinx (2010), LogiCORE IP Fast Fourier Transform v8.0, San Jose, CA, Xilinx, Inc. Available from: http://www.xilinx.com/support/documentation/ip_documentation/ds808_xfft.pdf [Accessed January 18, 2011].

Xin J, Donohue K D, Bilgutay N M and Li X (1991), 'Frequency diverse geometric mean filtering for ultrasonic flaw detection', *Materials Evaluation*, 987-992.

Yoon S, Oruklu E and Saniie J (2006), 'Dynamically reconfigurable neural network hardware design for ultrasonic target detection', *IEEE Ultrasonics Symposium*, 1377-1380.

Yoon S, Oruklu E and Saniie J (2007), 'Performance evaluation of neural network based ultrasonic flaw detection', *IEEE Ultrasonics Symposium*, 1579-1582.

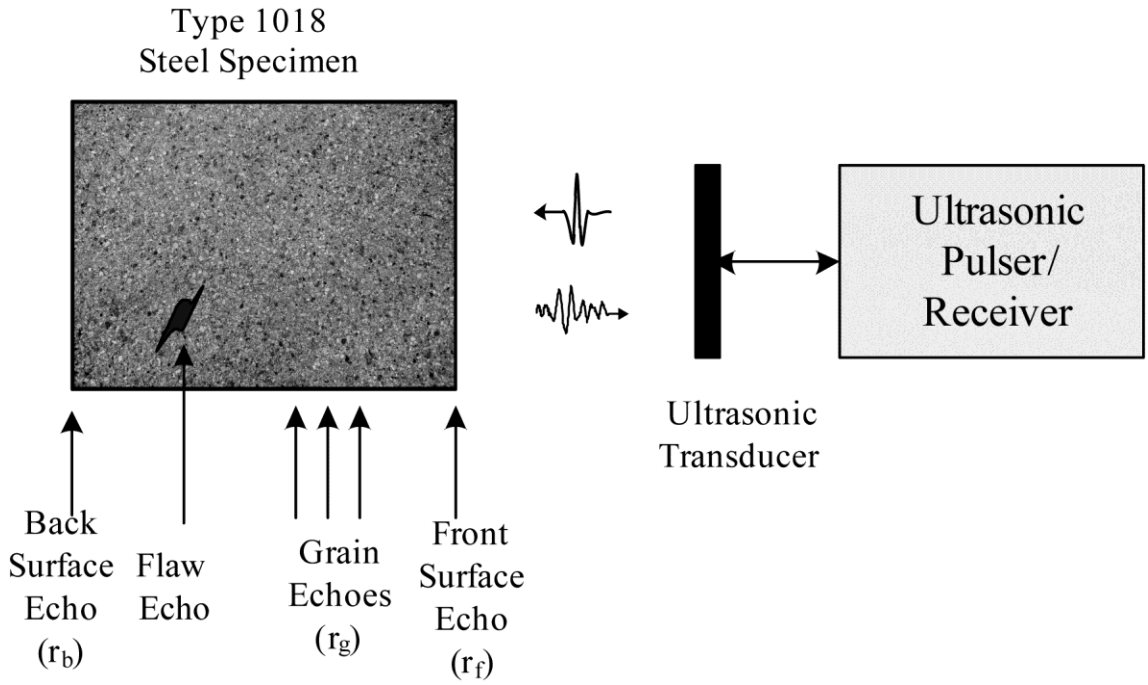

Fig. 1.1. Ultrasonic testing setup using a steel block (type 1018, grain size 50μm) to evaluate the characteristics of flaw echo and grain scattering.

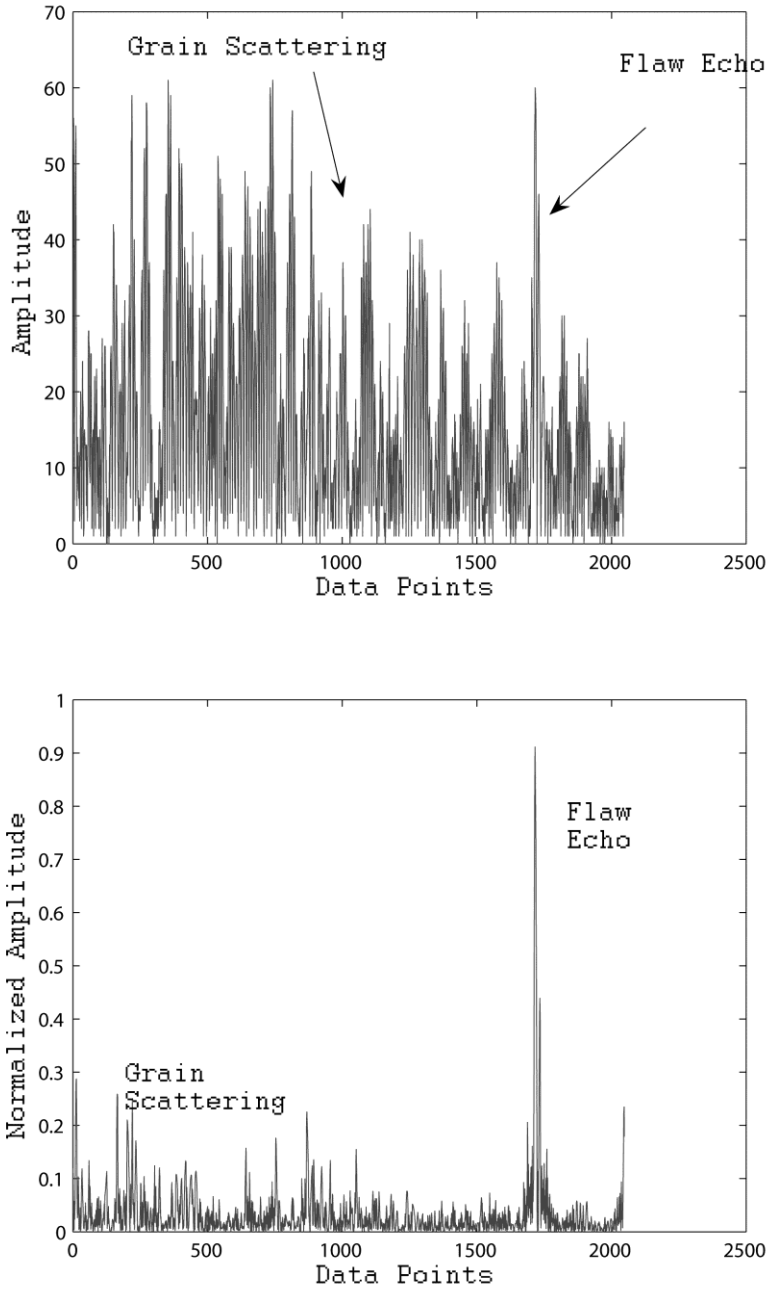

Fig. 1.2 Ultrasonic experimental flaw signal (top trace) and frequency-diverse minimum detector result (bottom trace). A broadband ultrasonic transducer with 5MHz center frequency and a pulser/receiver (Panametric, type 5052) operating in pulse-echo mode is used for the experimental measurement.

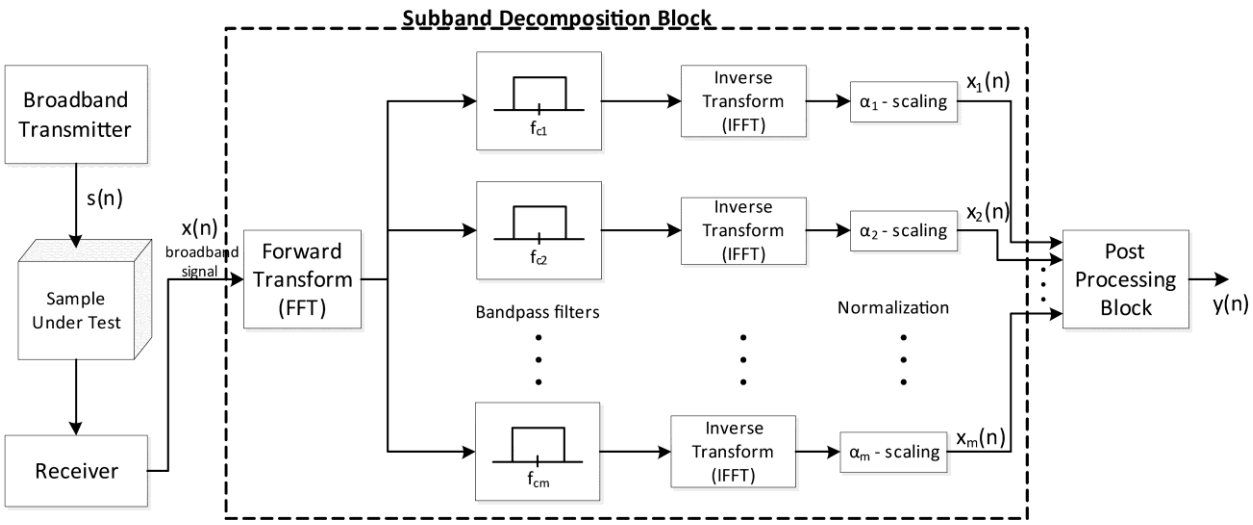

Fig. 1.3. Frequency-diverse ultrasonic flaw detection system based on split-spectrum processing

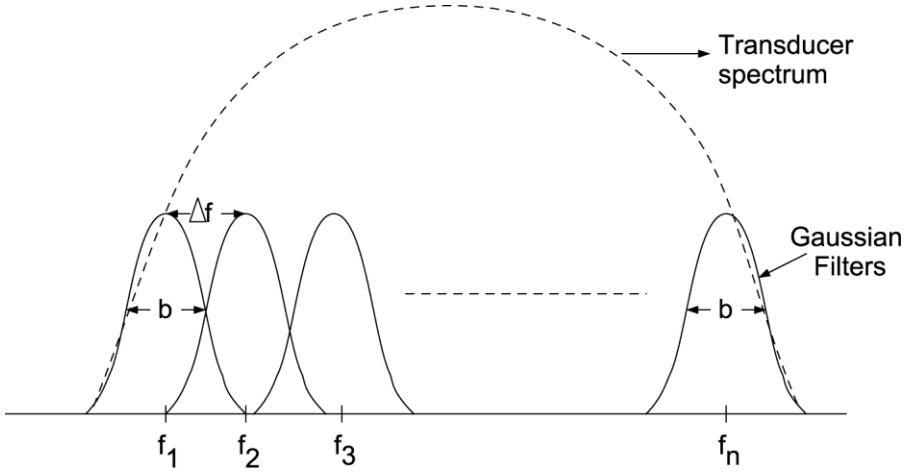

Fig. 1.4. Frequency bands in split-spectrum processing, where b is the filter bandwidth, Δf is the frequency step within the bands, and $f_1 \ldots f_n$ are the subbands' center frequency.

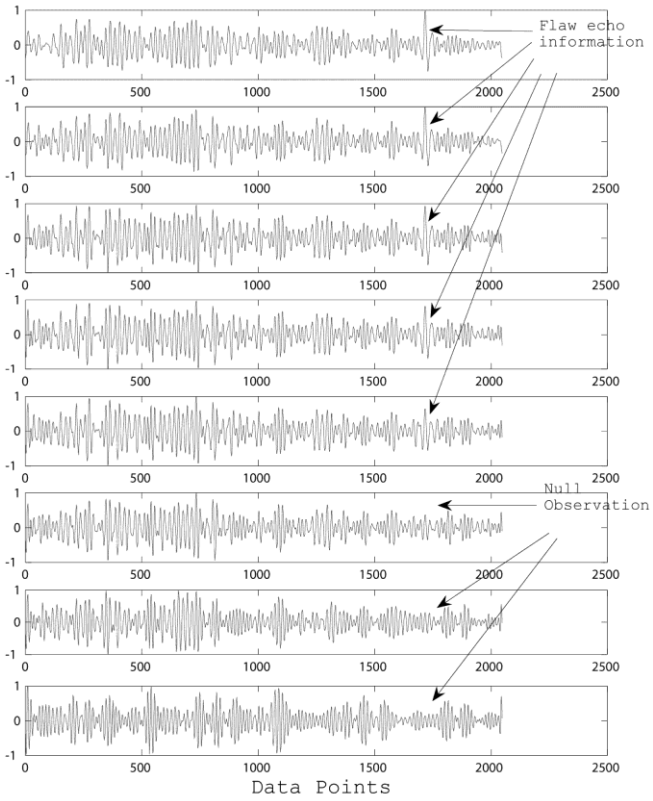

Fig. 1.5. Observation channels (output of split-spectrum processing) where the null observations are in higher frequency bands.

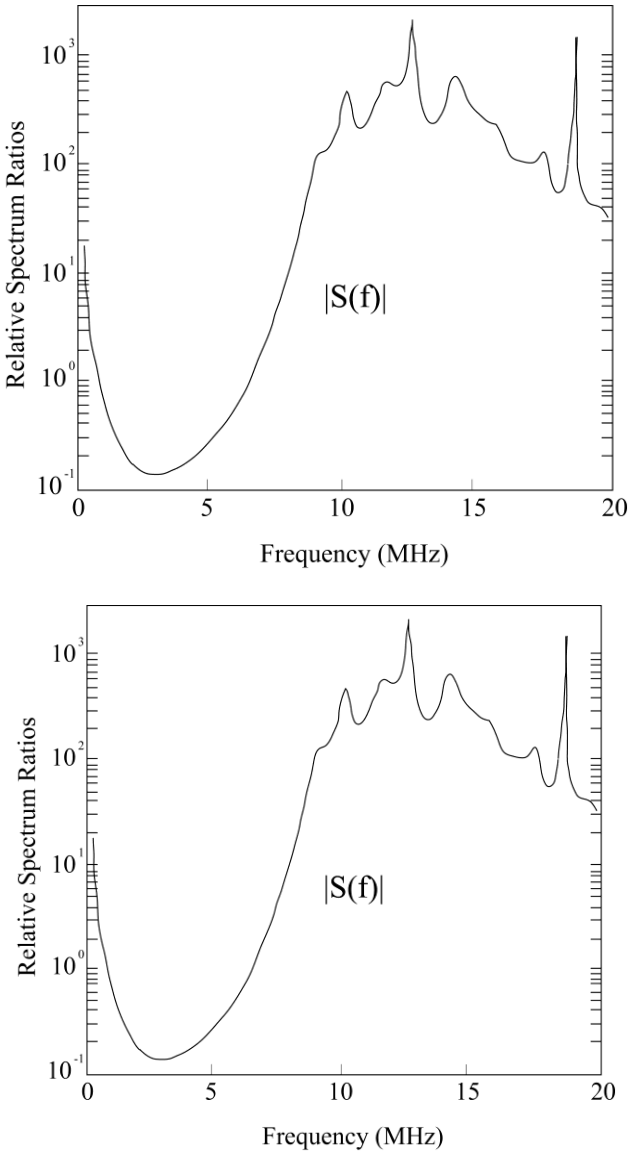

Fig. 1.6. a) Attenuation transfer function, b) Scattering transfer function

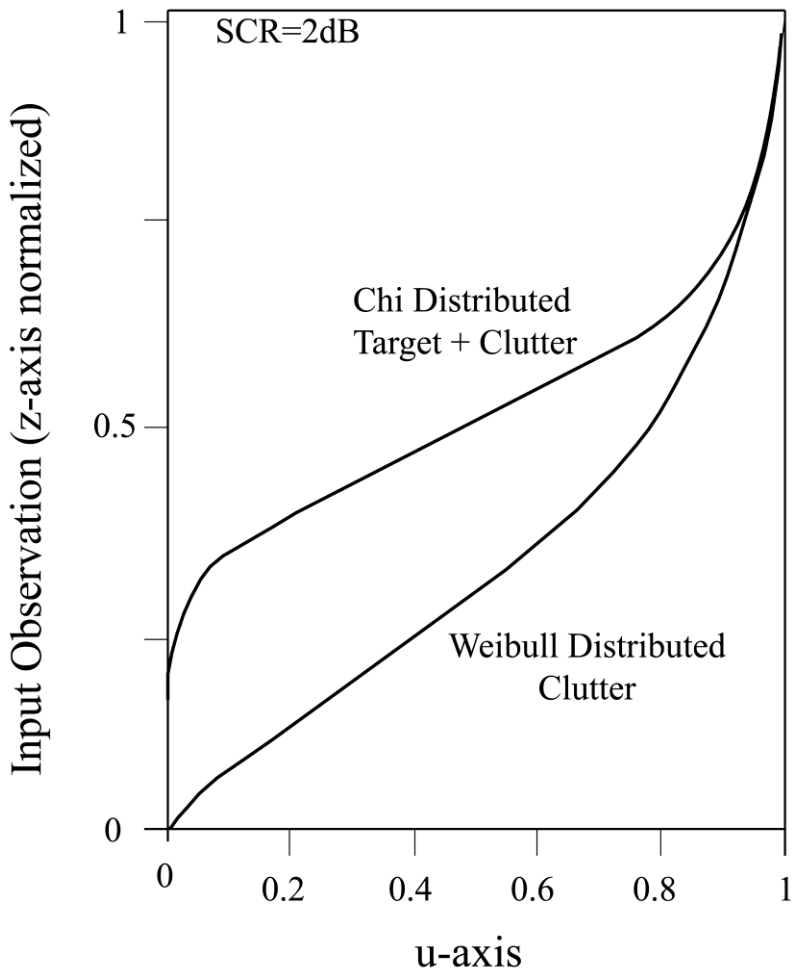

Fig. 1.7. Inverse distribution functions of Chi-distributed target-plus-clutter and Weibull-distributed clutter

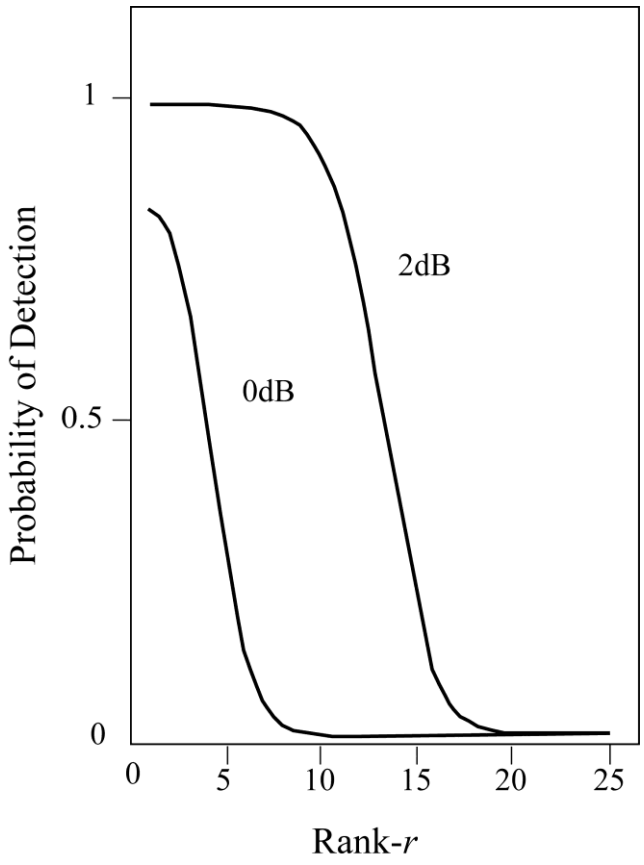

Fig. 1.8. Probability of detection of Chi distributed target-plus-clutter in Weibull distributed clutter for various ranks of OS filters with n =25 and the probability of false alarm set at 0.001

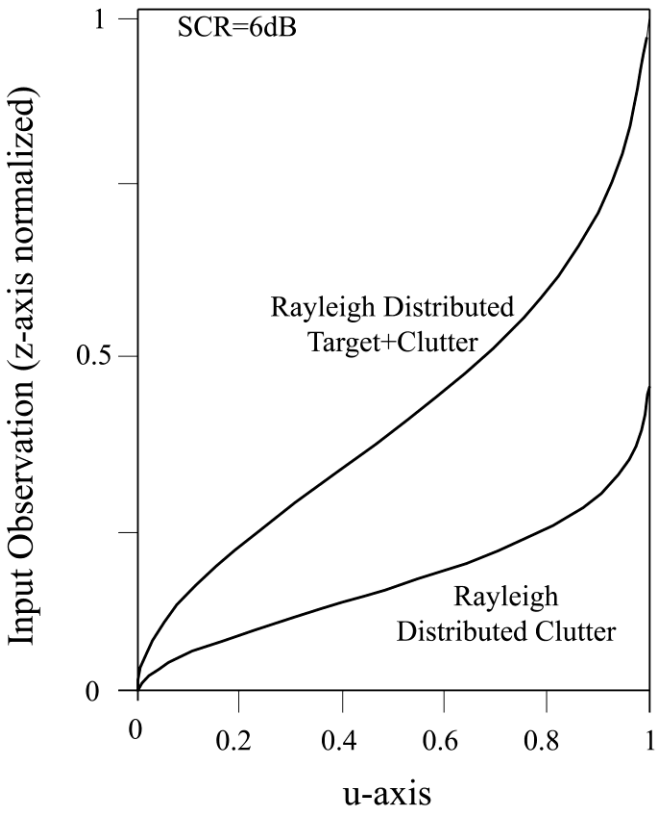

Fig. 1.9. Inverse distribution functions of Rayleigh-distributed target-plus-clutter and Rayleigh distributed clutter

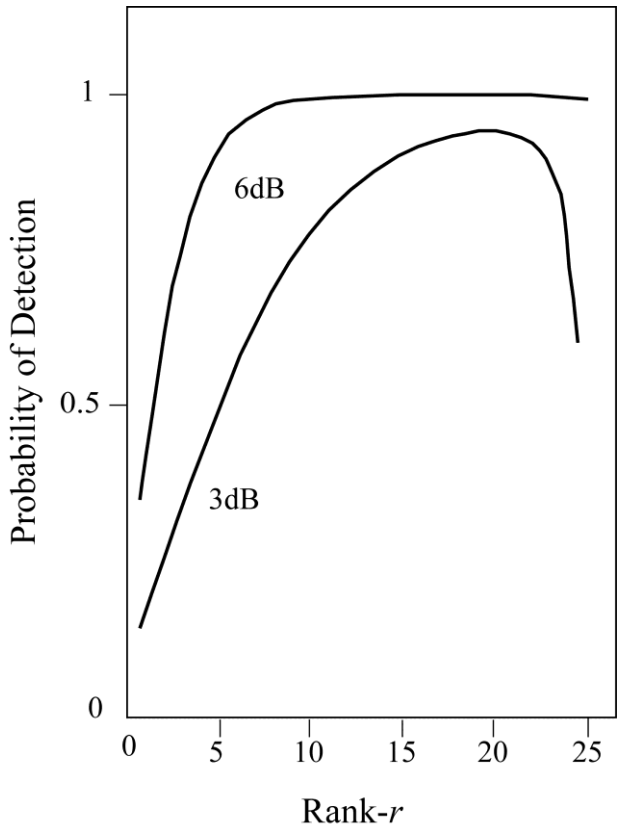

Fig. 1.10. Probability of detection of Rayleigh distributed target in Rayleigh distributed clutter for various ranks of OS filters with n =25 and the probability of false alarm set at 0.001.

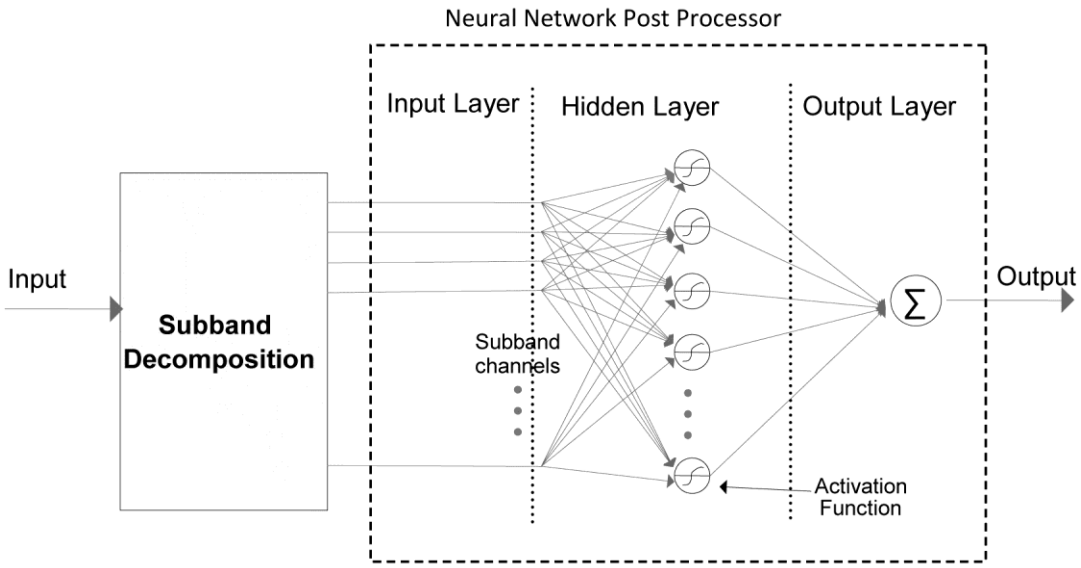

Fig. 1.11. Three layer feed-forward neural network for SSP flaw detection

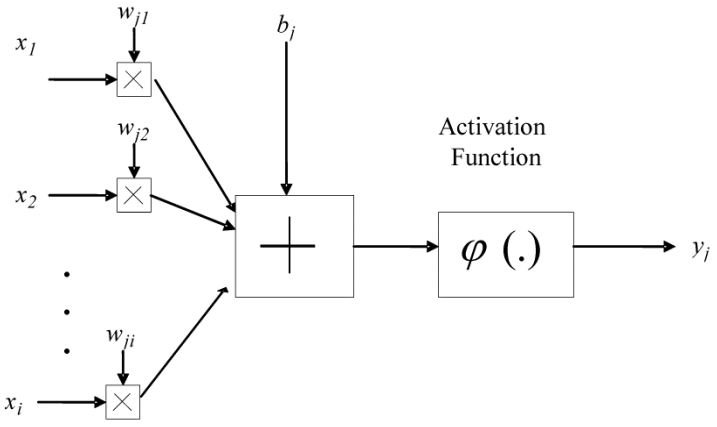

Fig. 1.12. Neural node model

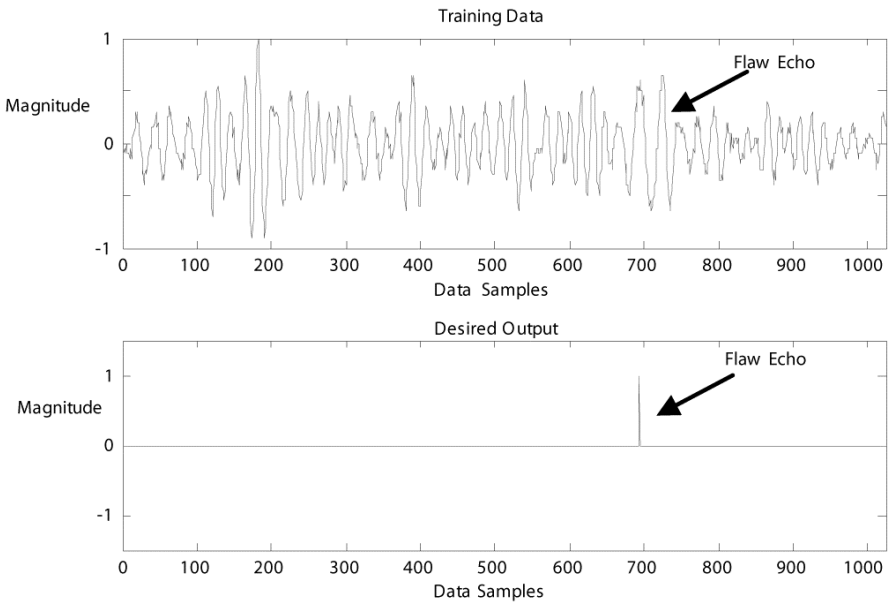

Fig. 1.13. Training data and desired neural network output

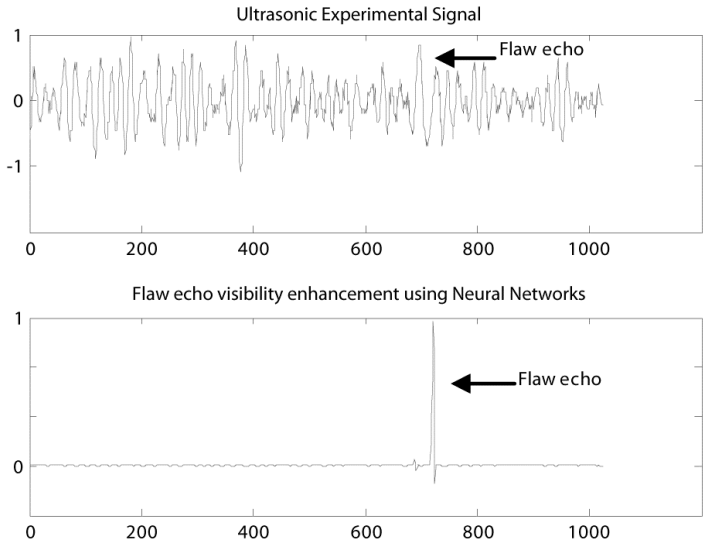

Fig. 1.14. Detection results using Neural Network based SSP

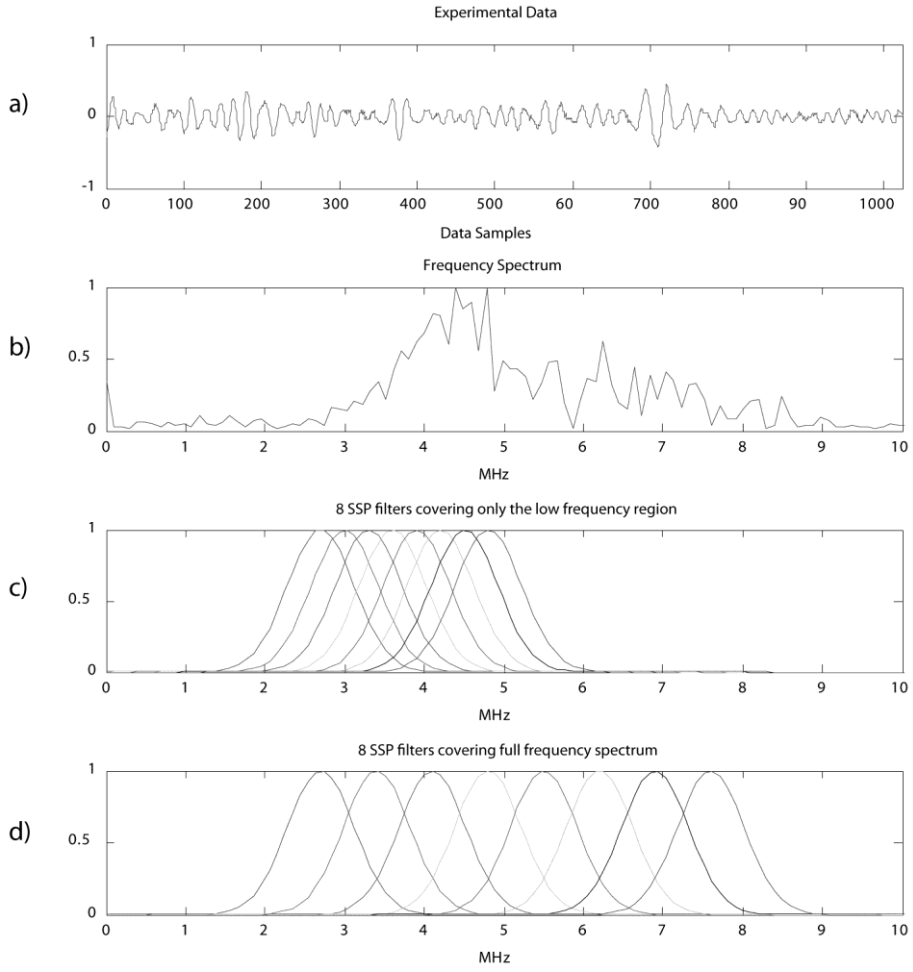

Fig. 1.15. Experimental data in time domain, frequency domain and frequency bands of SSP filters

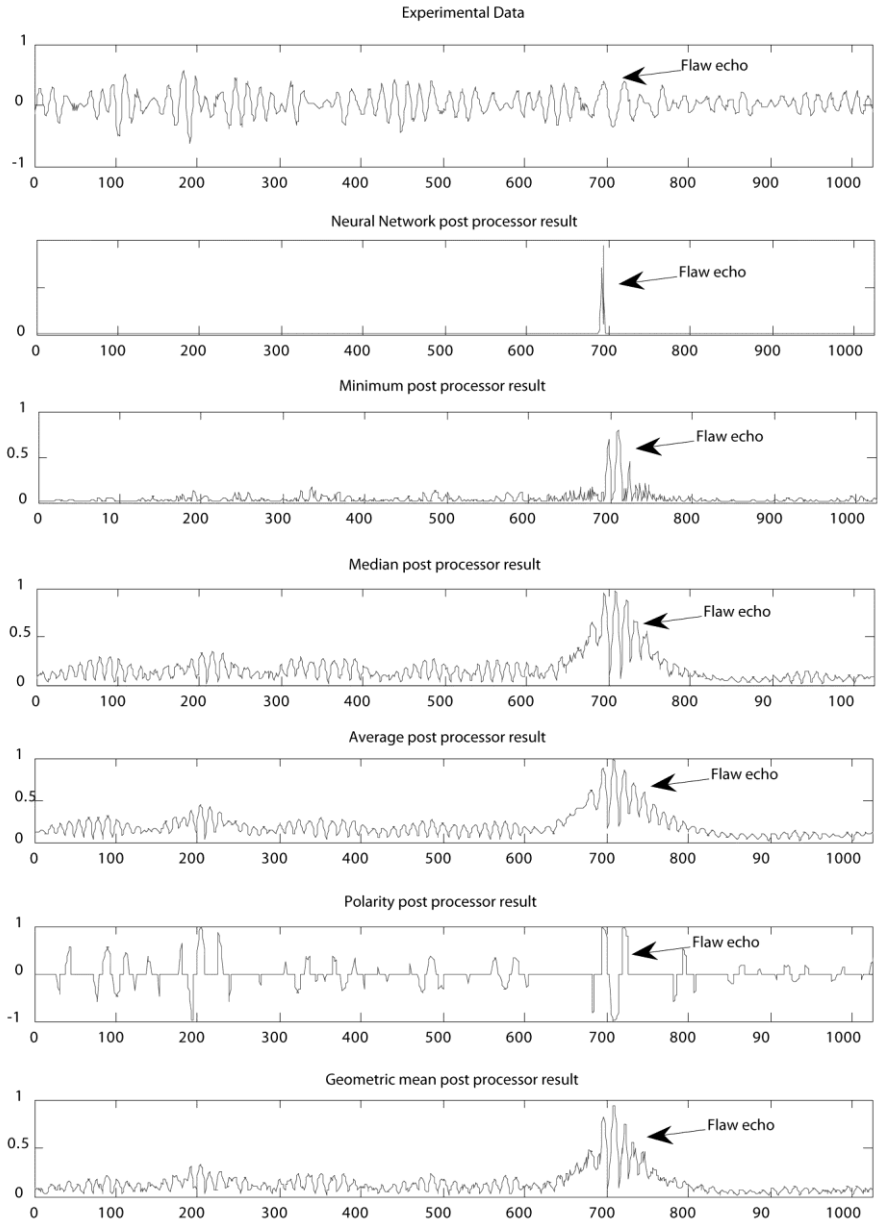

Fig. 1.16. Comparison of detection results when SSP channels covering the low frequency region

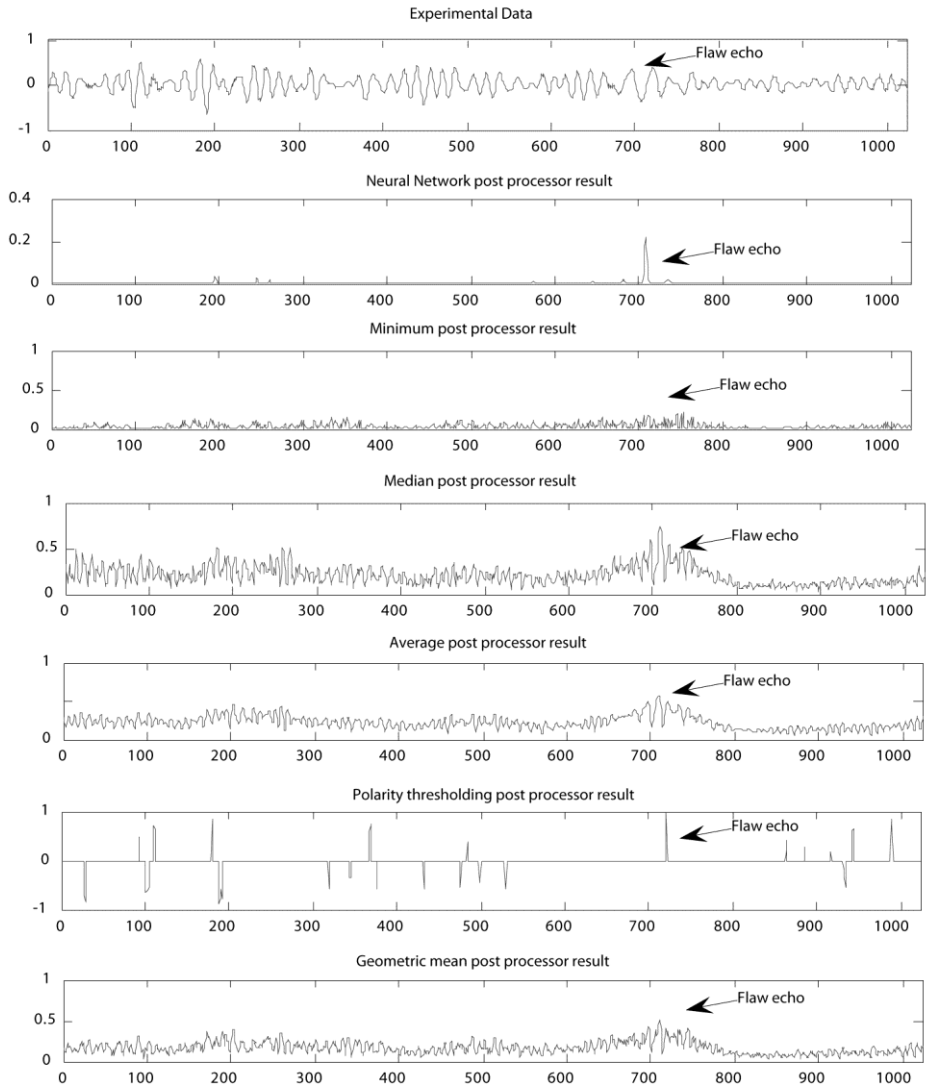

Fig. 1.17. Comparison of detection results when SSP channels covering the full frequency range

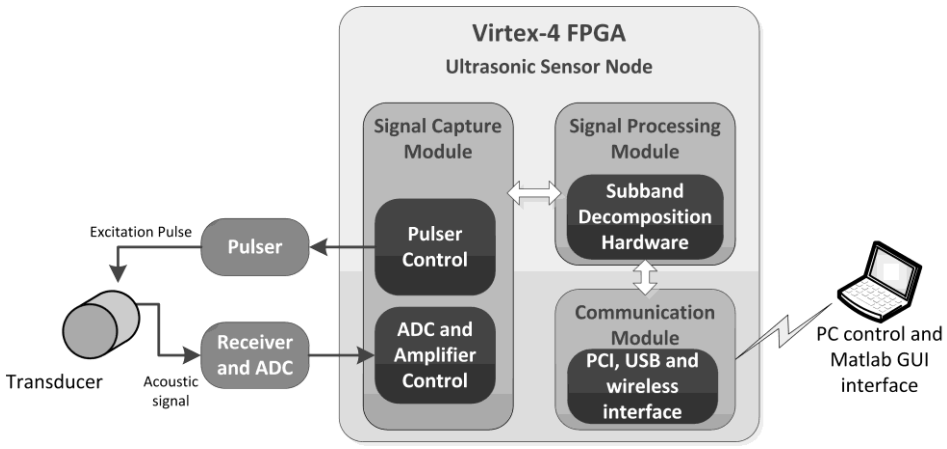

Fig. 1.18. FPGA based real-time ultrasonic flaw detection system

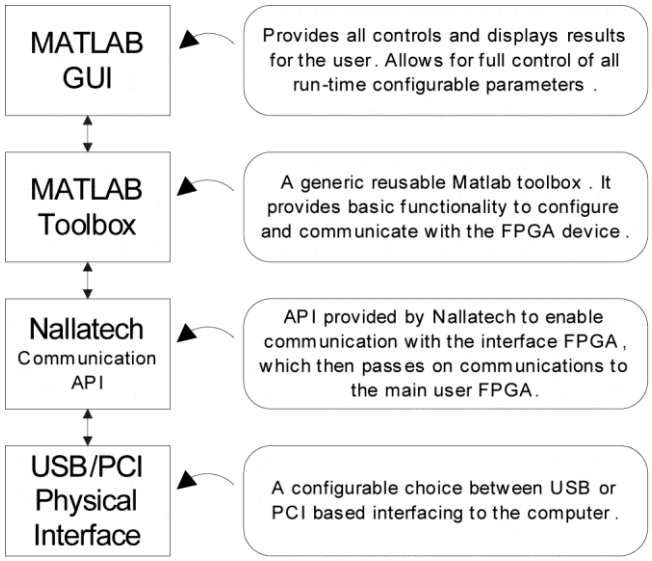

Fig. 1.19. Software interface designed for ultrasonic flaw detection system

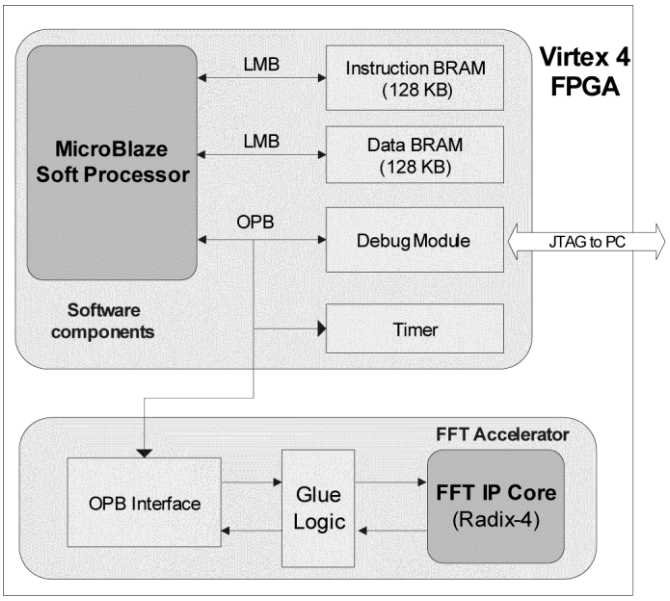

Fig. 1.20. Hardware/Software co-design components

Table 1.1 FCR enhancement of various ultrasonic target detectors (average of multiple measurements)

Input FCR	Neural Networks Detector	Minimum Detector	Median Detector	Average Detector	Geometric Mean Detector	Polarity Threshold Detector
SSP filters covering only the low frequency range of the signal						
1.1 dB	46.8 dB	7.9 dB	7.1 dB	5.0 dB	7.0 dB	0 dB
SSP filters covering the full frequency range of the signal						
1.1 dB	23.7 dB	1.7 dB	1.0 dB	1.4 dB	1.5 dB	0.3 dB

Table 1.2 Comparison of FCR improvement using different hardware and software (HW/SW) co-design techniques using minimum detector

Data set	Input FCR (dB)	Software Implementation 4-channel (db)	Software Implementation 8-channel (db)	HW/SW Co-Design 4-channel (dB)	Hardware Radix-2 4-channel (dB)	Hardware Radix-2 8-channel (dB)
1	3.69	6.50	8.91	8.96	3.02	11.90
2	-2.33	15.80	17.12	15.46	12.31	13.20
3	2.24	12.67	11.96	9.67	8.73	8.90
4	-3.74	16.36	17.44	14.00	10.11	13.30
5	0.00	10.39	12.18	10.53	7.31	9.95
6	1.54	10.22	9.89	7.24	7.43	8.78
7	2.69	11.10	13.77	9.08	8.49	10.29
8	4.14	7.21	12.31	9.99	5.50	10.78
9	4.25	8.38	7.35	4.44	0.87	7.44
10	-1.70	10.27	10.42	11.43	10.48	12.39
Average	1.07	10.89	12.14	10.08	7.43	10.69

Table 1.3 Processing time of the SSP algorithm

Algorithm Stage	Software without FPU (Cycles)	Software with FPU (Cycles)	HW/SW Codesign with FFT Accelerator (Cycles)	Hardware only (Radix-2 FFT IP-core) (cycles)	Hardware only (Radix-4 FFT IP-core) (cycles)
FFT	28,764,300	599,026	3,456	5,190	1,322
Bandpass filtering	98,884	99,153	91,456	1,024	1,024
Inverse FFT	109,978,539	2,396,039	13,824	5,190	1,322
Post Processing	1,086,792	66,169	196,661	1,024	1,024
Total Cycles	140,540,767	3,772,536	305,397	12,428	4,692
Total Execution Time	1,405.5ms	37.7ms	3.05ms	108μs	40.8μs

Table 1.4 FPGA resource usage for implementing SSP

	Software Architecture without FPU	Software architecture with FPU	HW/SW Co-Design	Hardware Architecture (4-channel)	Hardware Architecture (8-channel)
Slices	1307	1886	5836	8378	14505
DSP48	3	7	25	30	54
RAM16	35	35	39	28	48