ECE 429 – Introduction to VLSI Design

Credits: 4, **Contact Hours:** Two 75 minute lecture session per week, one 160 minute laboratory session per week.

Coordinator: J. Wang, Associate Professor of ECE

Textbook: Neil H.E. Weste and David Harris, *CMOS VLSI DESIGN: A Circuits and Systems Perspective*, 4th ed., Addison-Wesley, 2010.

2019 Catalog Data: ECE 429: Introduction to VLSI Design. Credit 4.
Processing, fabrication, and design of Very Large Scale Integration (VLSI) circuits. MOS transistor theory, VLSI processing, circuit layout, layout design rules, layout analysis, and performance estimation. The use of computer aided design (CAD) tools for layout design, system design in VLSI, and application-specific integrated circuits (ASICs). In the laboratory, students create, analyze, and simulate a number of circuit layouts as design projects, culminating in a term design project. (3-3-4) (P) (C)

Prerequisites or co-requisites by topic: ECE 218, ECE 311, senior standing.

Enrollment: Elective course for EE majors; hardware-design elective course for CPE majors.

Specific outcomes of instruction:
After completing this course, the student should be able to do the following:

1. Design VLSI circuits from register-transfer level to layouts.
2. Discuss the basic attributes of VLSI systems, their impact upon society, and the tradeoffs between design metrics, especially speed, power, and cost.
3. Design experiments to measure design metrics and explain the differences between theoretical models and experiments.
4. Identify the basic parts of VLSI design flows. Compare/contrast both custom and standard-cell based design methodologies.
5. Explain and analyze dynamic techniques such as charge sharing and current leakage and how it impacts specific circuits from a dynamic circuits perspective.
6. Complete an engineering design incorporating engineering standards and realistic constraints.
7. Prepare an informative and organized design project report with solid supporting data and deliver an oral presentation.

Relationship of ECE 429 specific outcomes of instruction to student outcomes:

	Student Outcomes	**Course Goals**
1	An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics	1,2,3,4,5,6
2	An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors	1,6
3	An ability to communicate effectively with a range of audiences	7
4	An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts	2
5	An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives	6,7
6	An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions	3,6
7	An ability to acquire and apply new knowledge as needed, using appropriate learning strategies	

Topics:

- MOS Transistor Theory (1 week)
- CMOS Fabrication, Layout, Processing Technology (1 week)
- Logical Effort (1 week)
- Delay and Power Estimation for CMOS (1 week)
- Interconnect and wire engineering (1 week)
- Simulation in HSPICE and Verilog (1 week)
- Combinational Circuit Design (1.5 week)
- Sequential Circuit Design (1.5 week)
- Adders (1.5 week)
- Datapath Functional Units (1 week)
- Memories (1 week)
- Final project and Demonstration (1 weeks)
- Midterm and Final Exams (1.5 weeks)

Laboratory topics:

- Lab Setup (1 week)
- Inverter Schematic (1 week)
- Inverter Layout (1 week)
- Gate Delay and Power (1 week)
- Hierarchical Design and Formal Verification (1 week)
- Carry-Ripple Addition I (1 week)
- Carry-Ripple Addition II (1 week)
- Carry-Ripple Addition III (1 week)
- ASIC Design Flow (1 week)
- Final Project: Design and Synthesis of Central Processing Units (4 weeks)

Prepared by: J. Wang **Date:** February 28, 2020